

FIG. 1

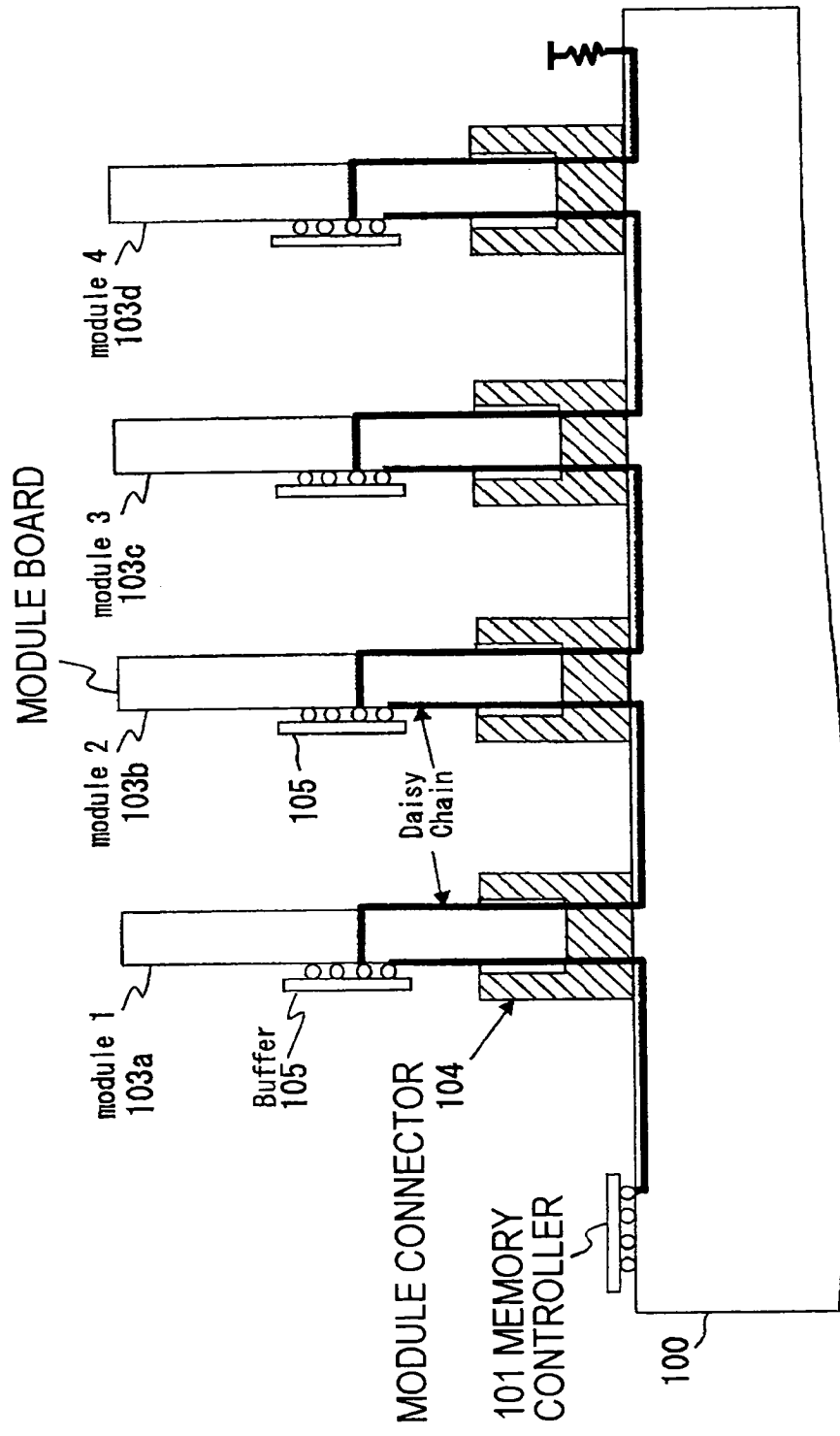
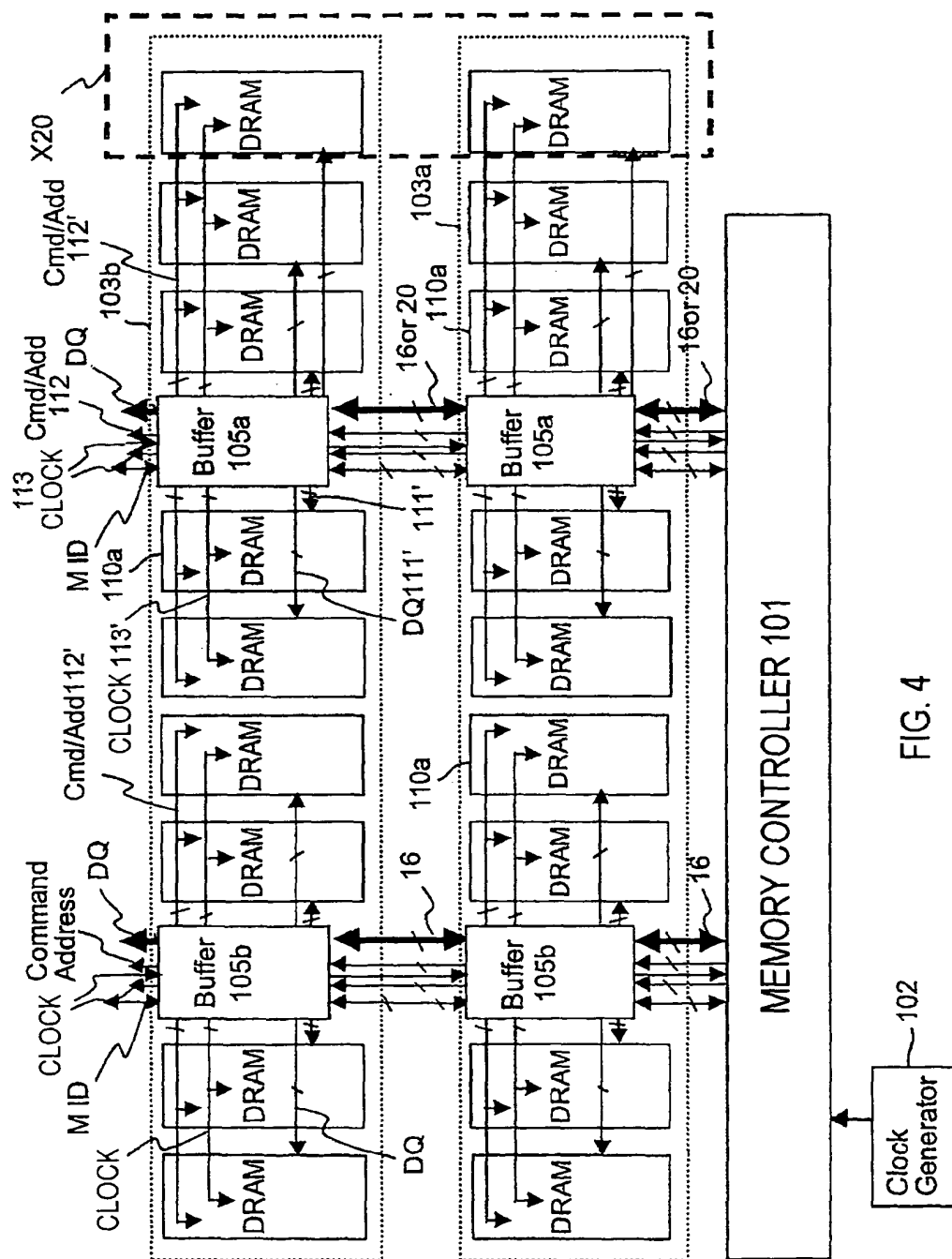


FIG. 3



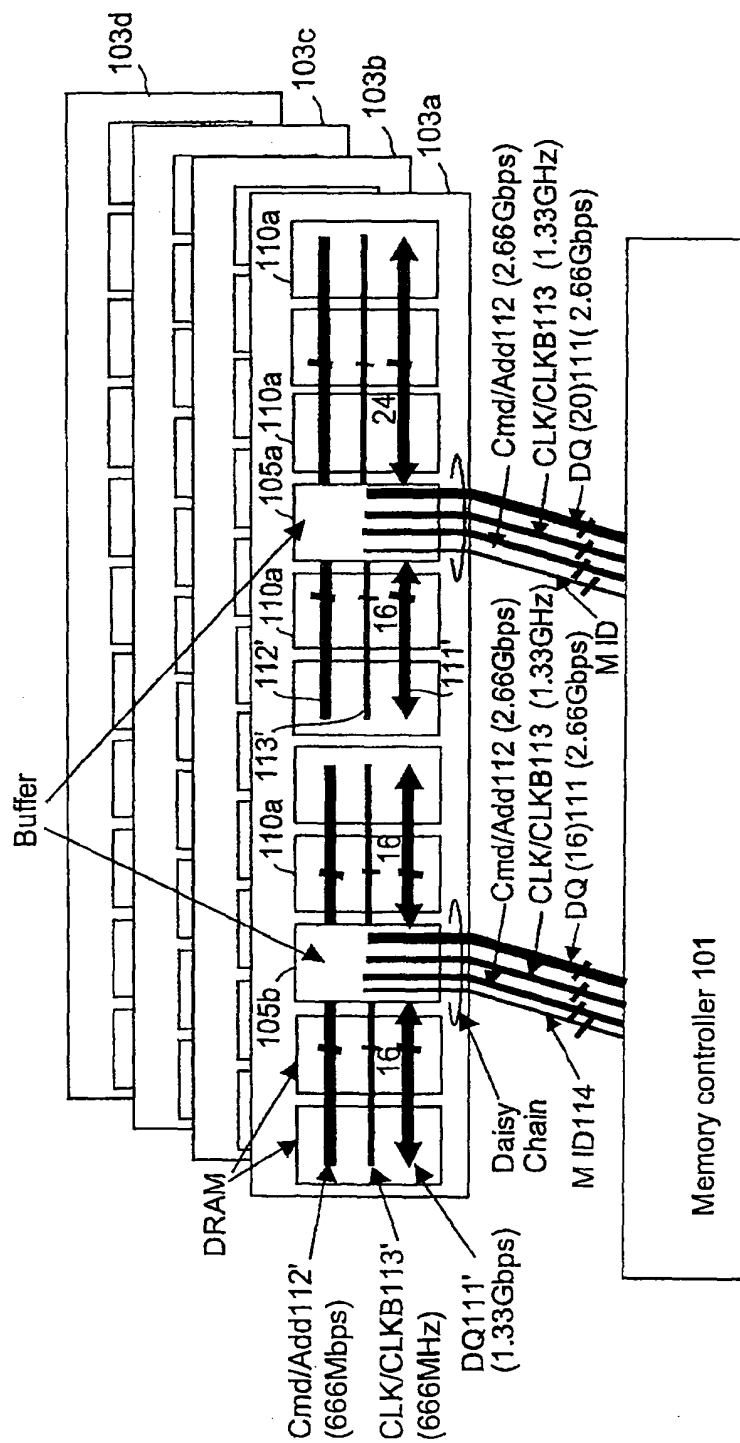


FIG. 5

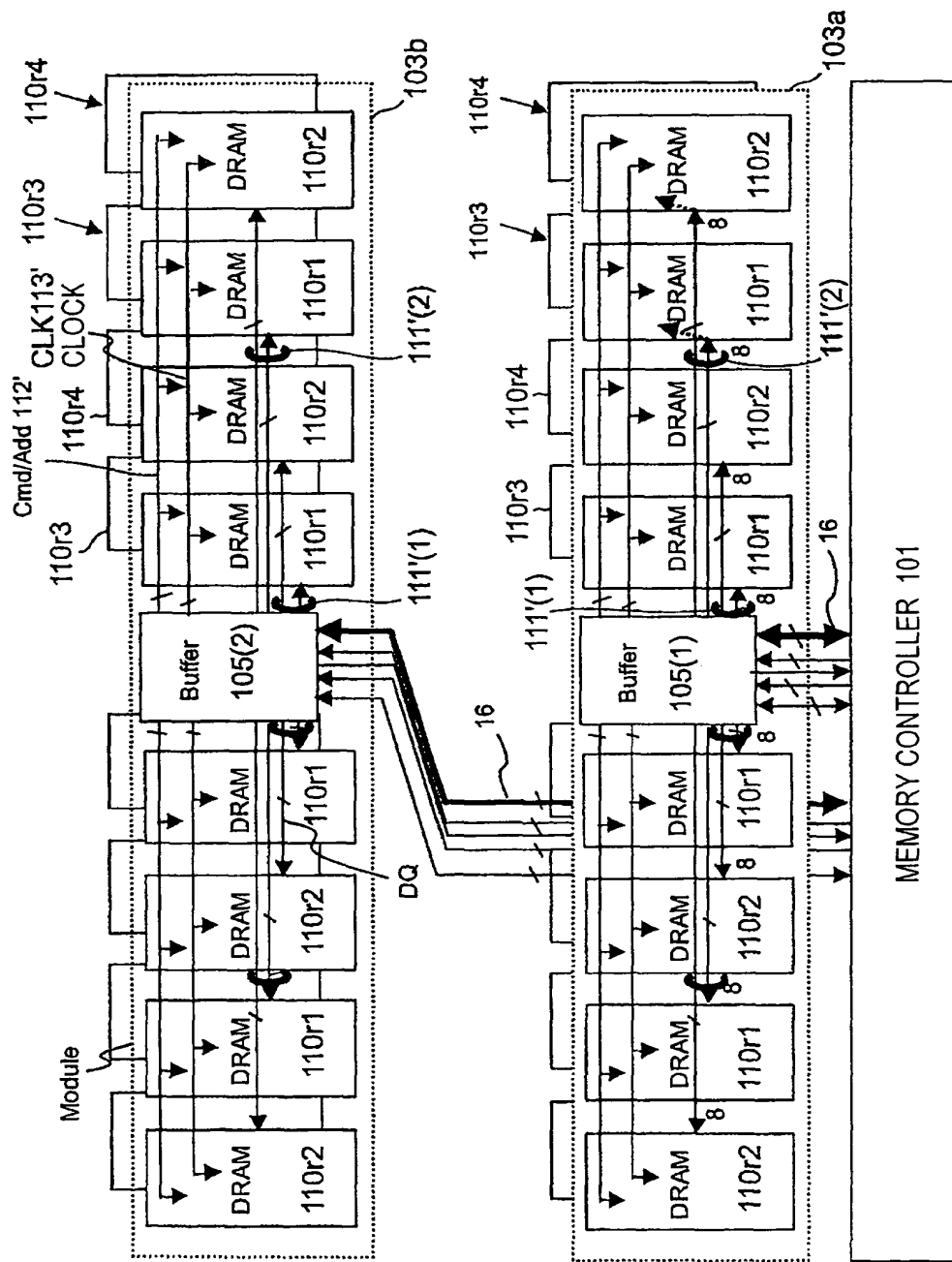
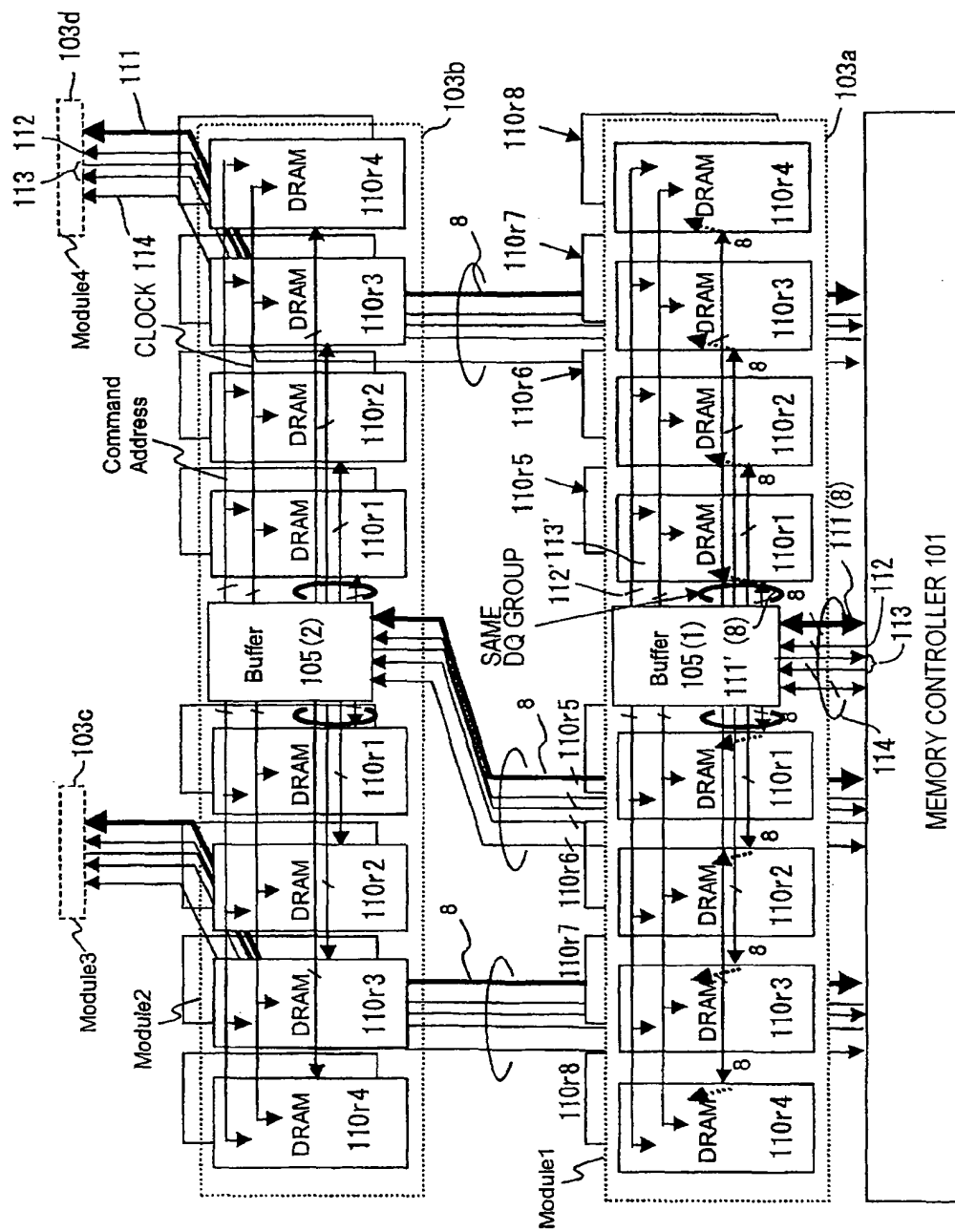


FIG. 7



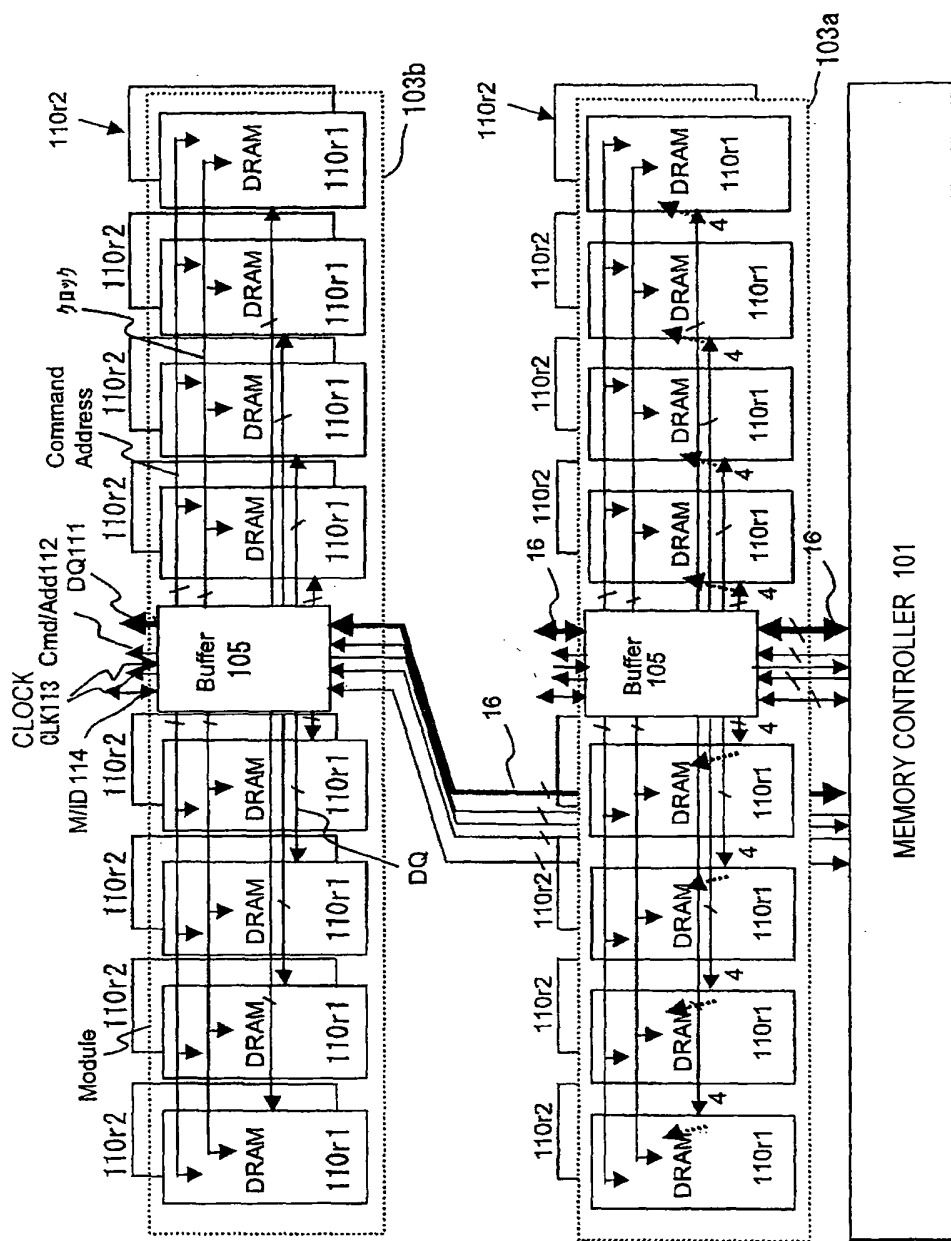


FIG. 9

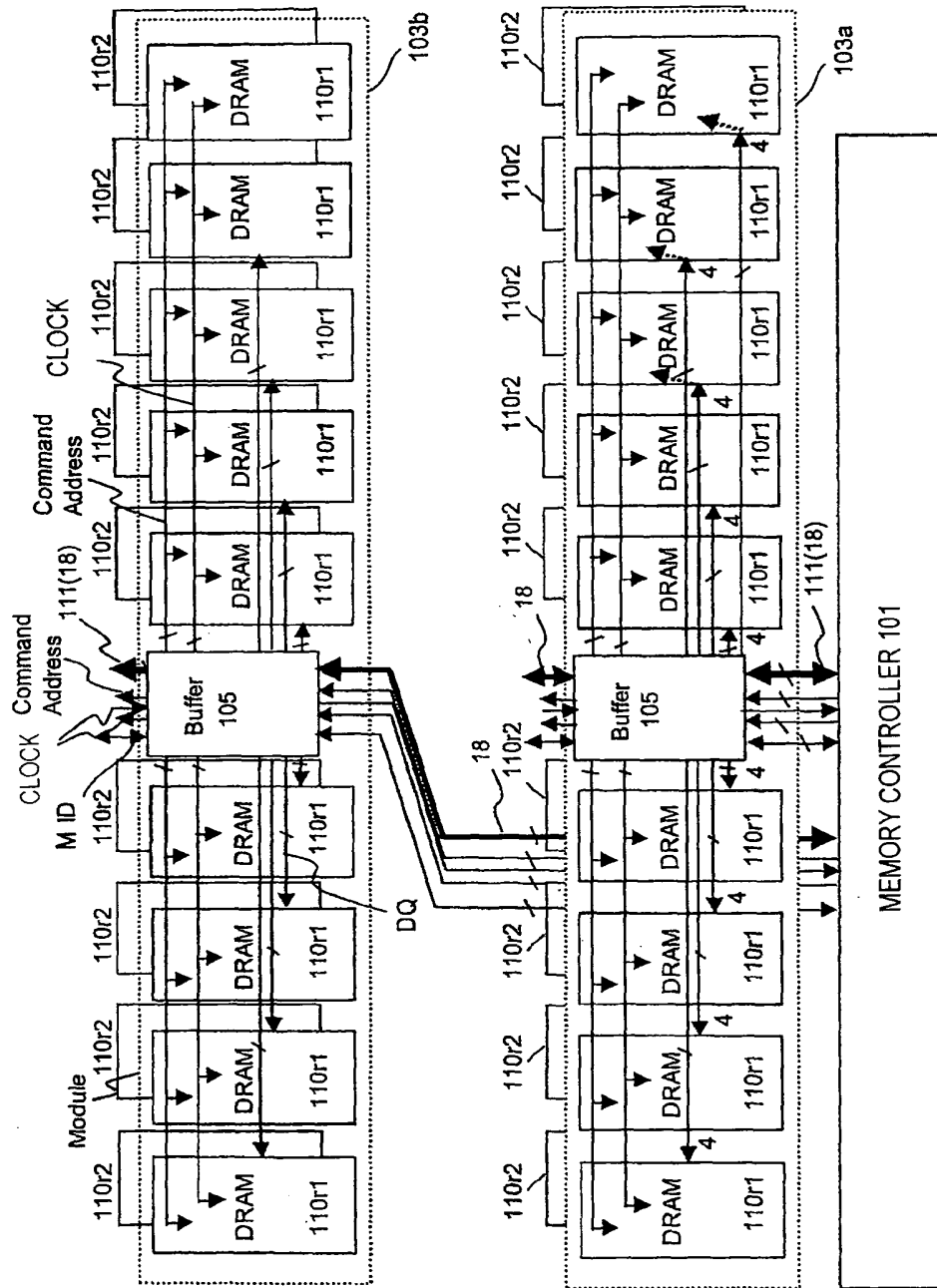


FIG. 10

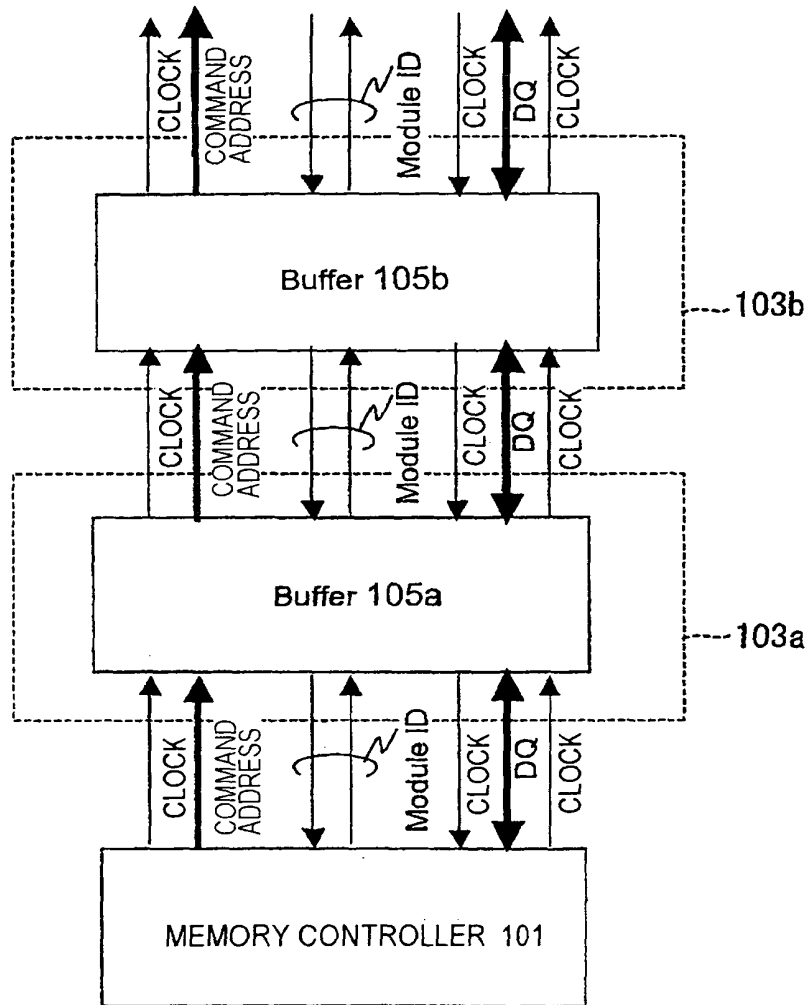


FIG. 11

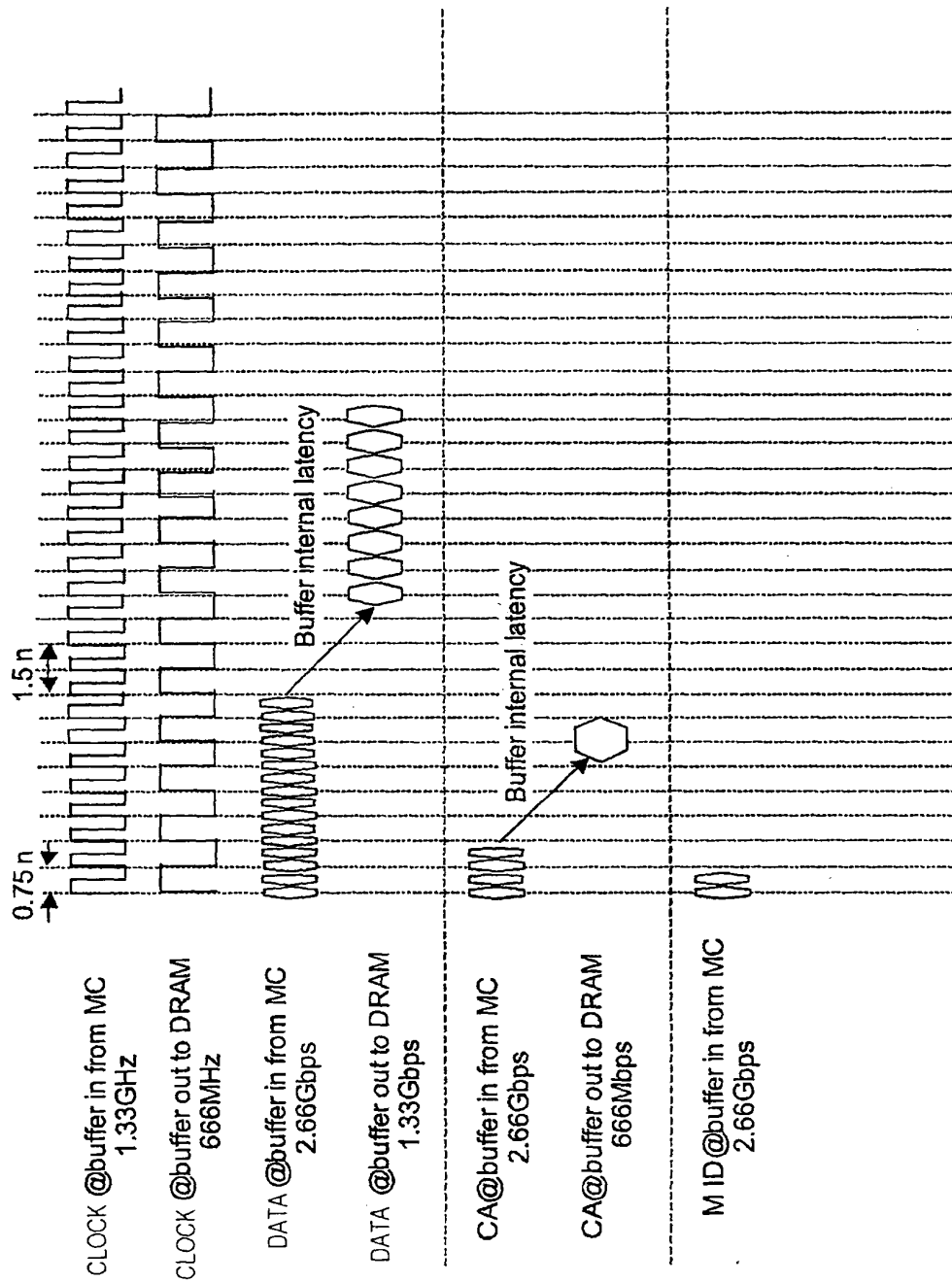


FIG. 12

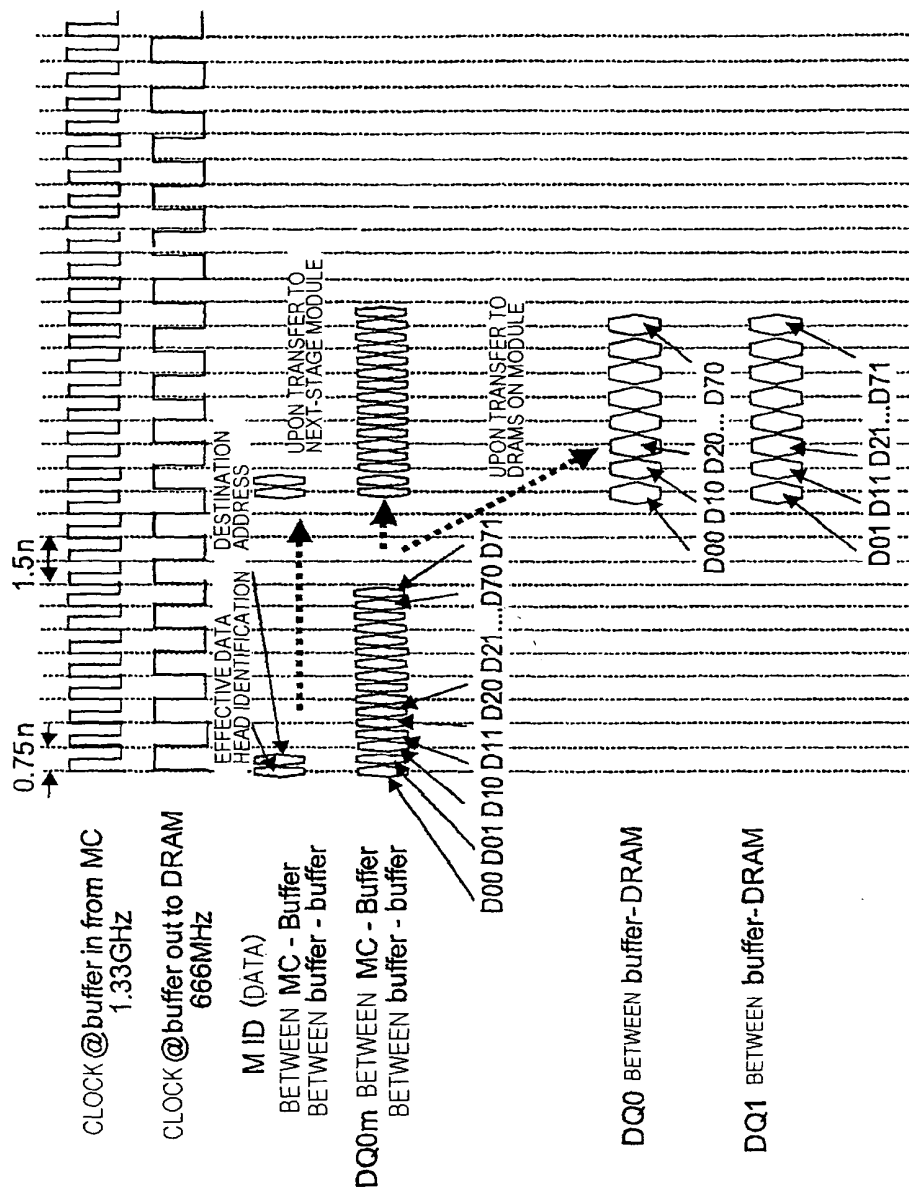


FIG. 13

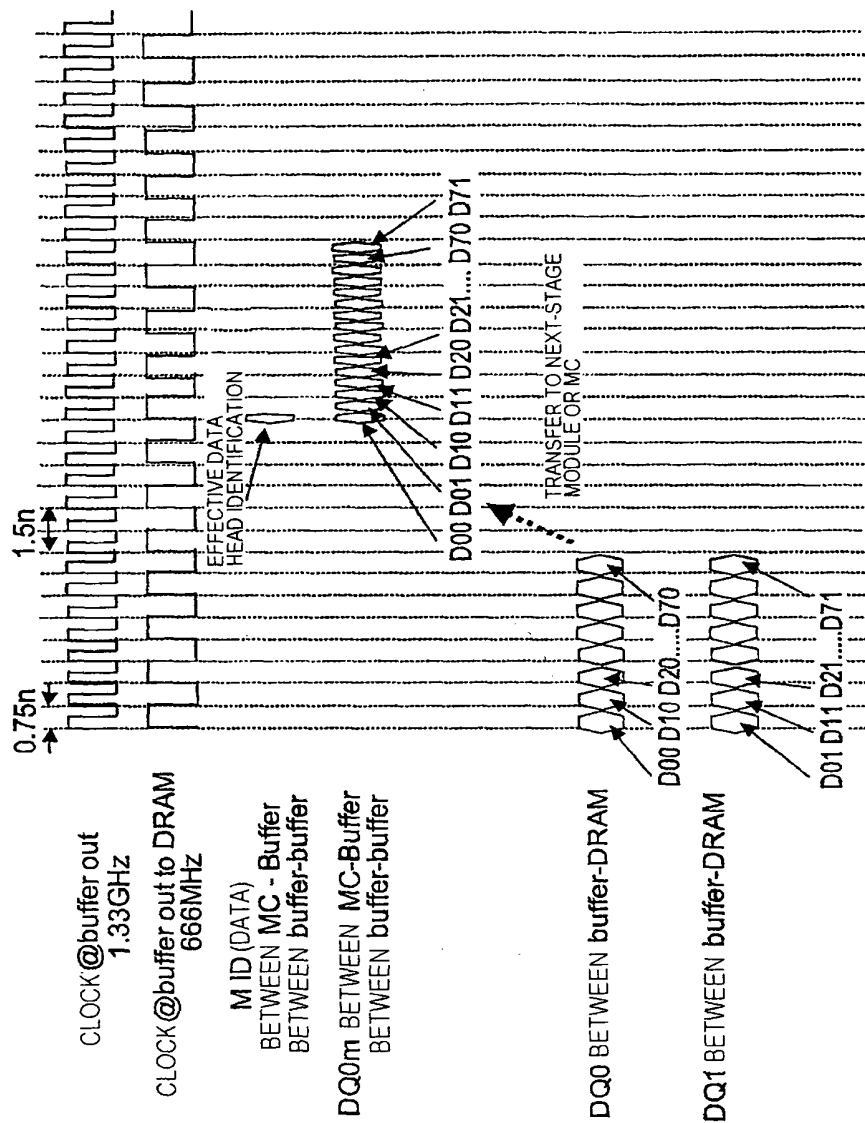


FIG. 14

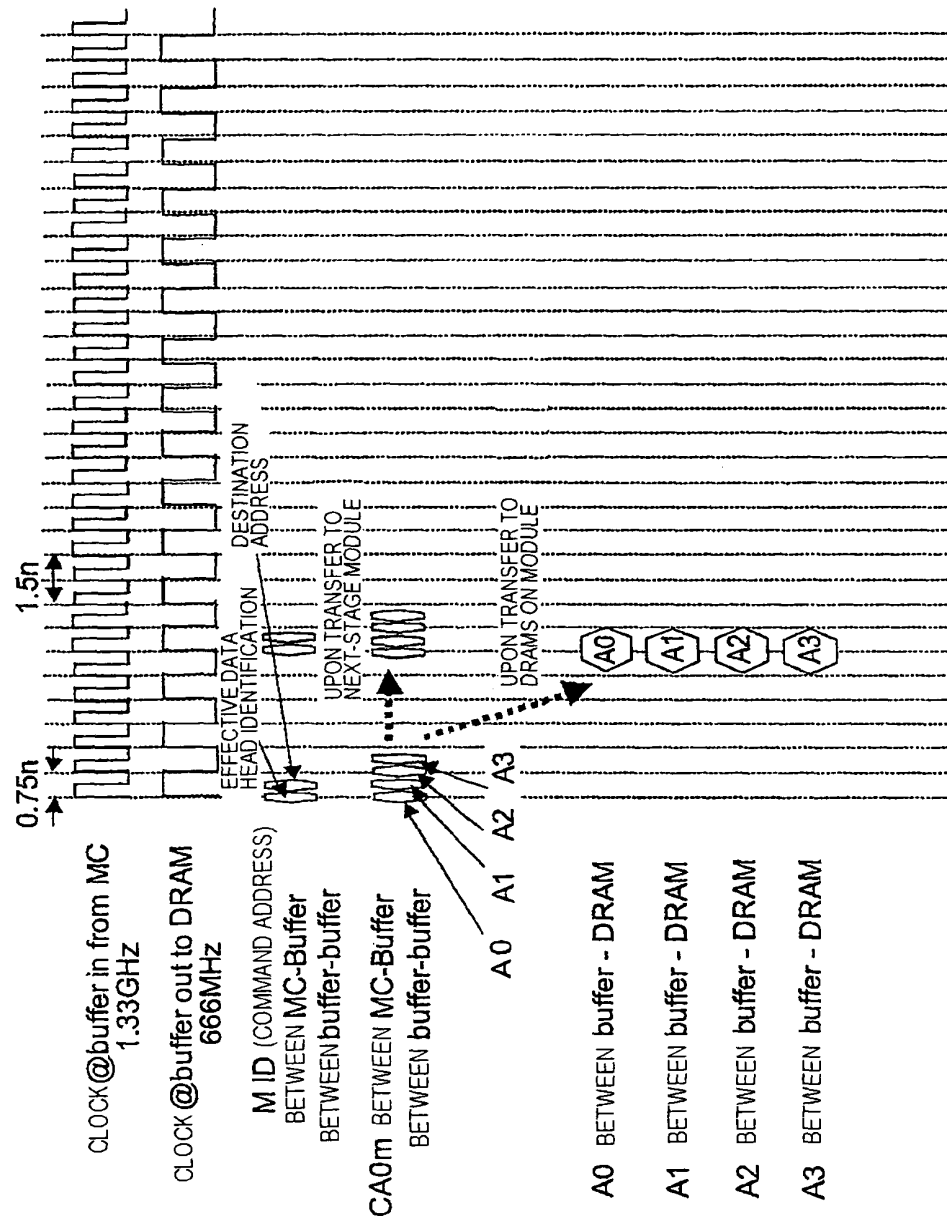


FIG. 15

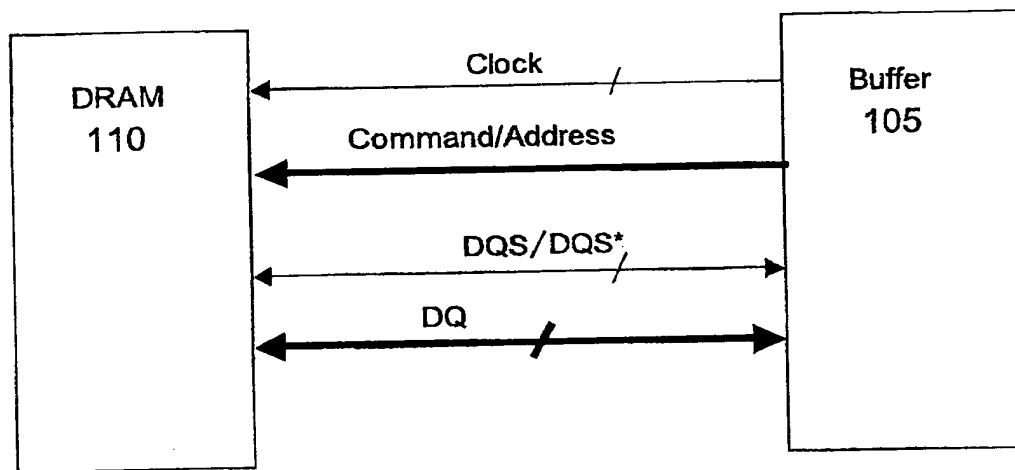


FIG. 16

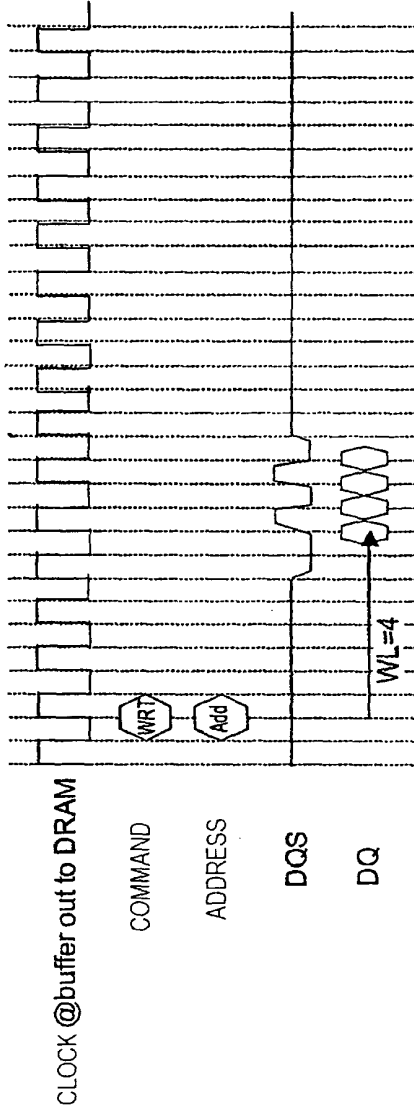


FIG. 17A

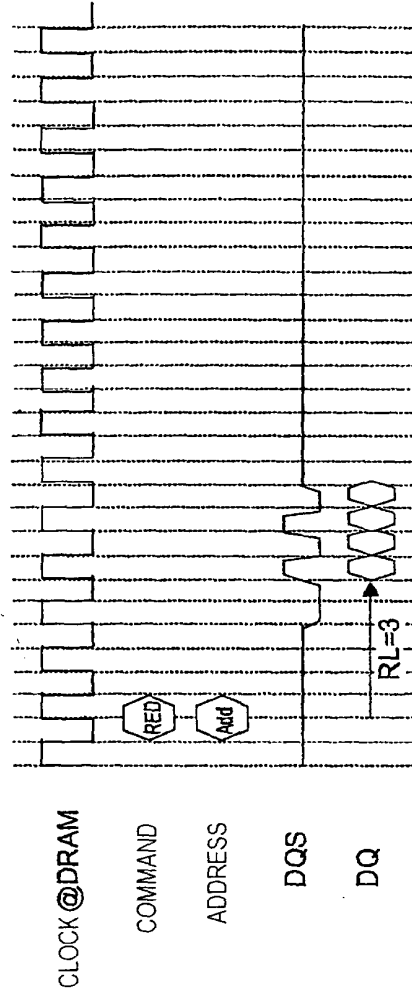


FIG. 17B

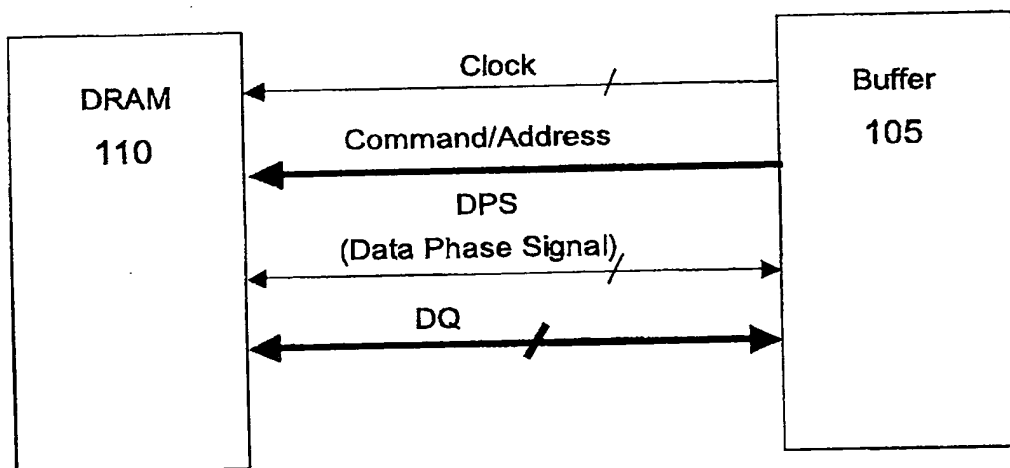


FIG. 18

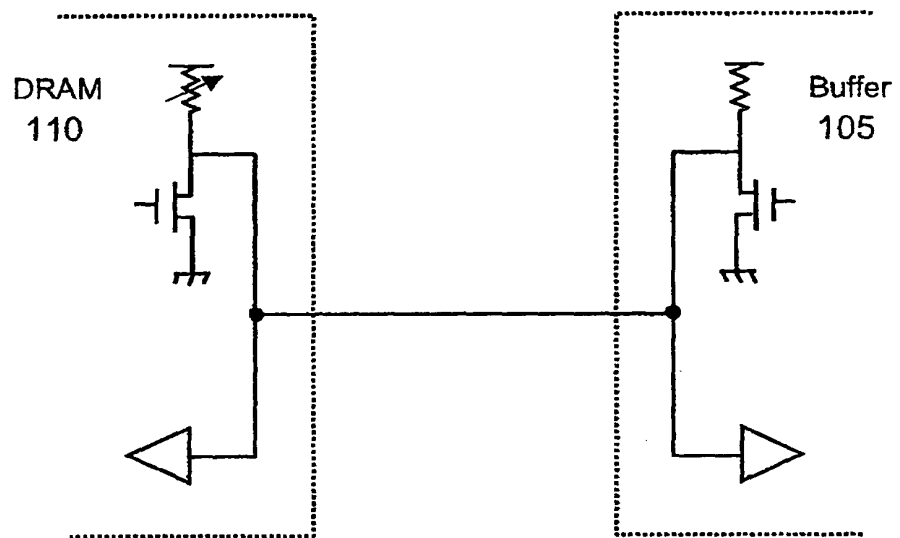


FIG. 19

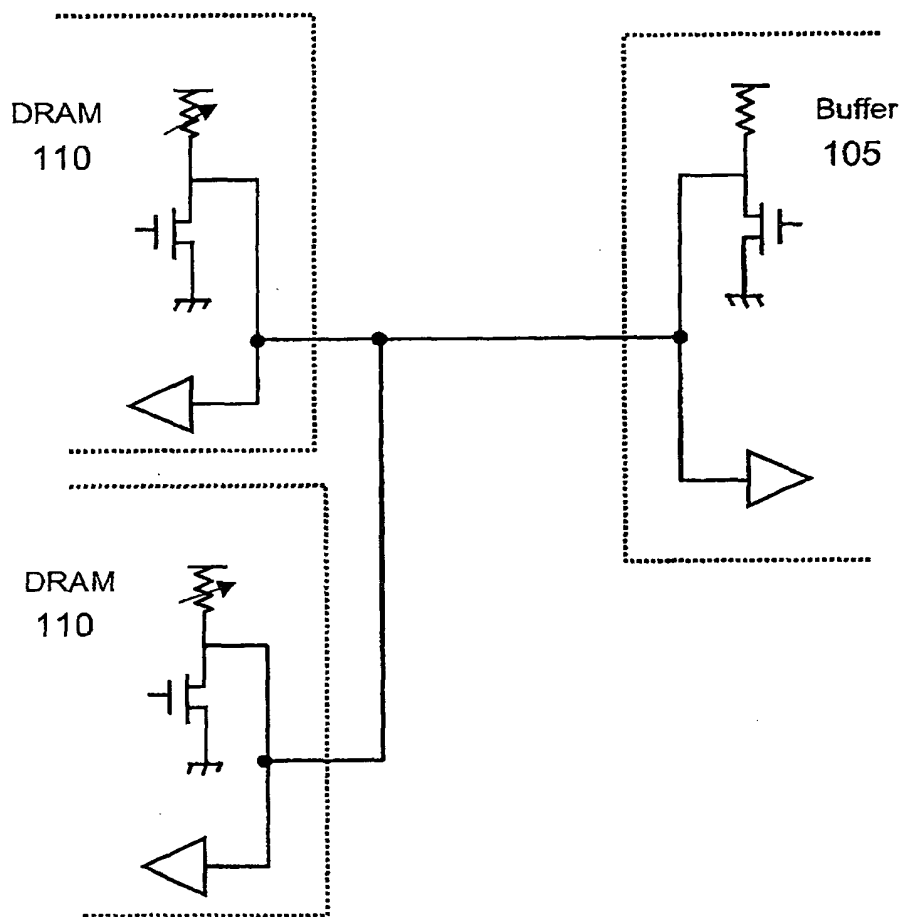


FIG. 20

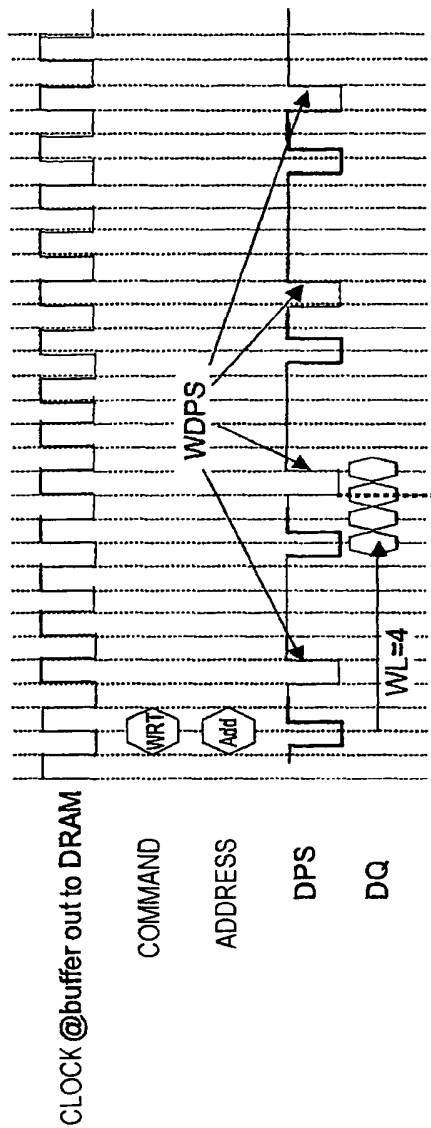


FIG. 21A

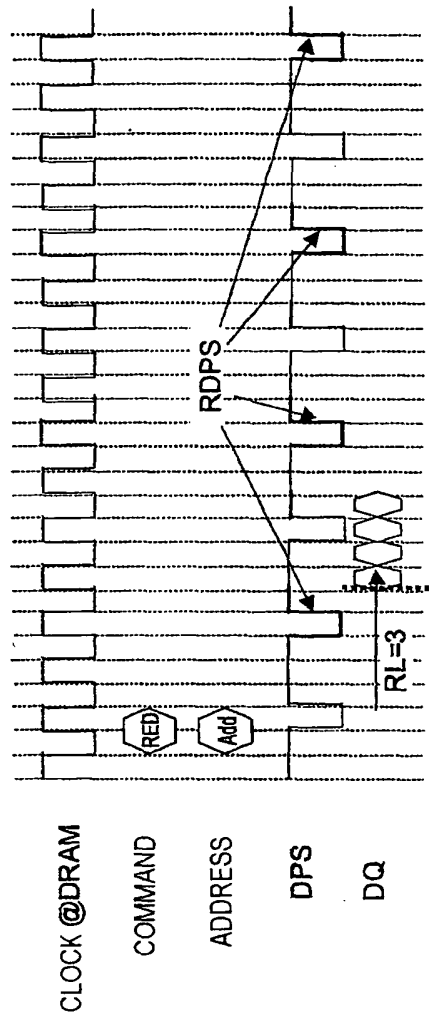


FIG. 21B

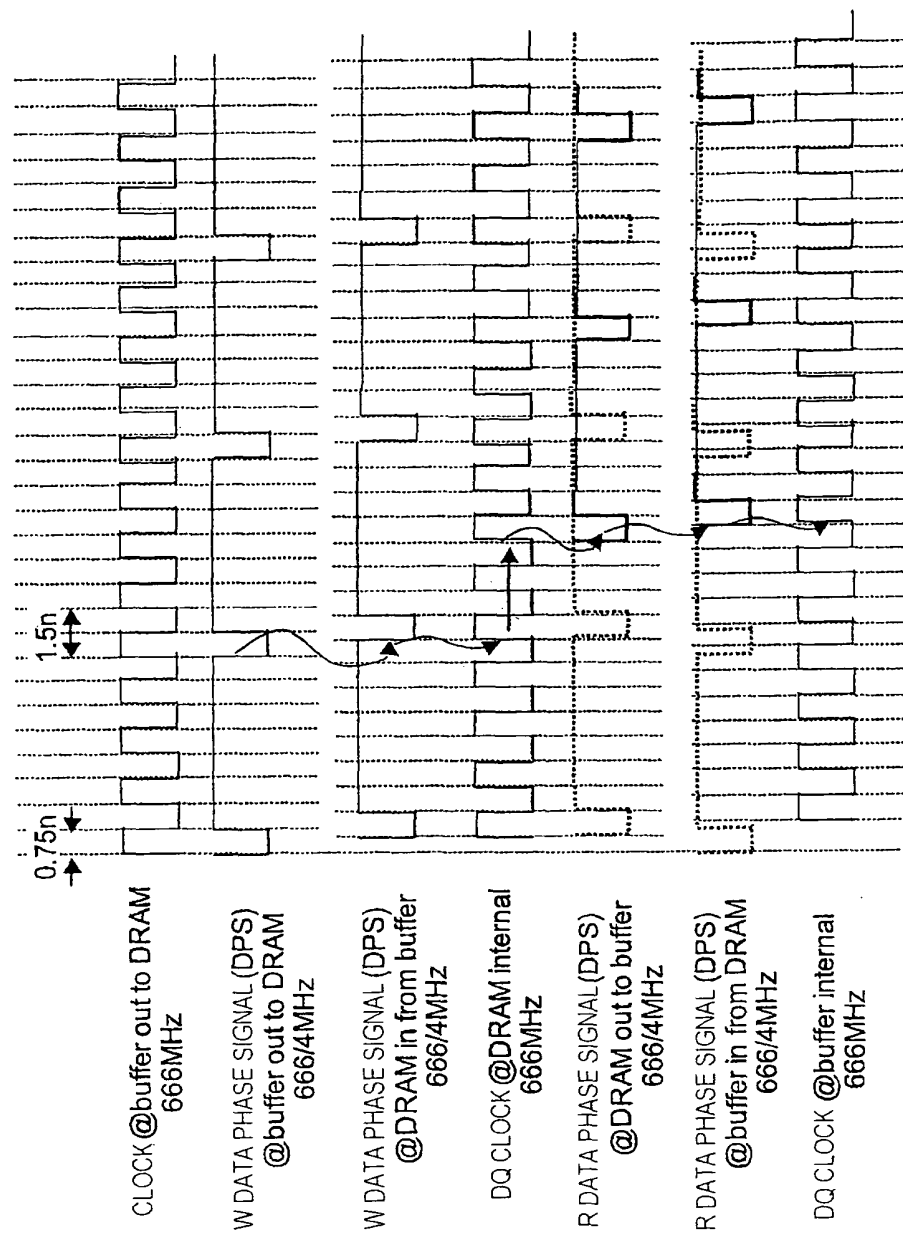


FIG. 22

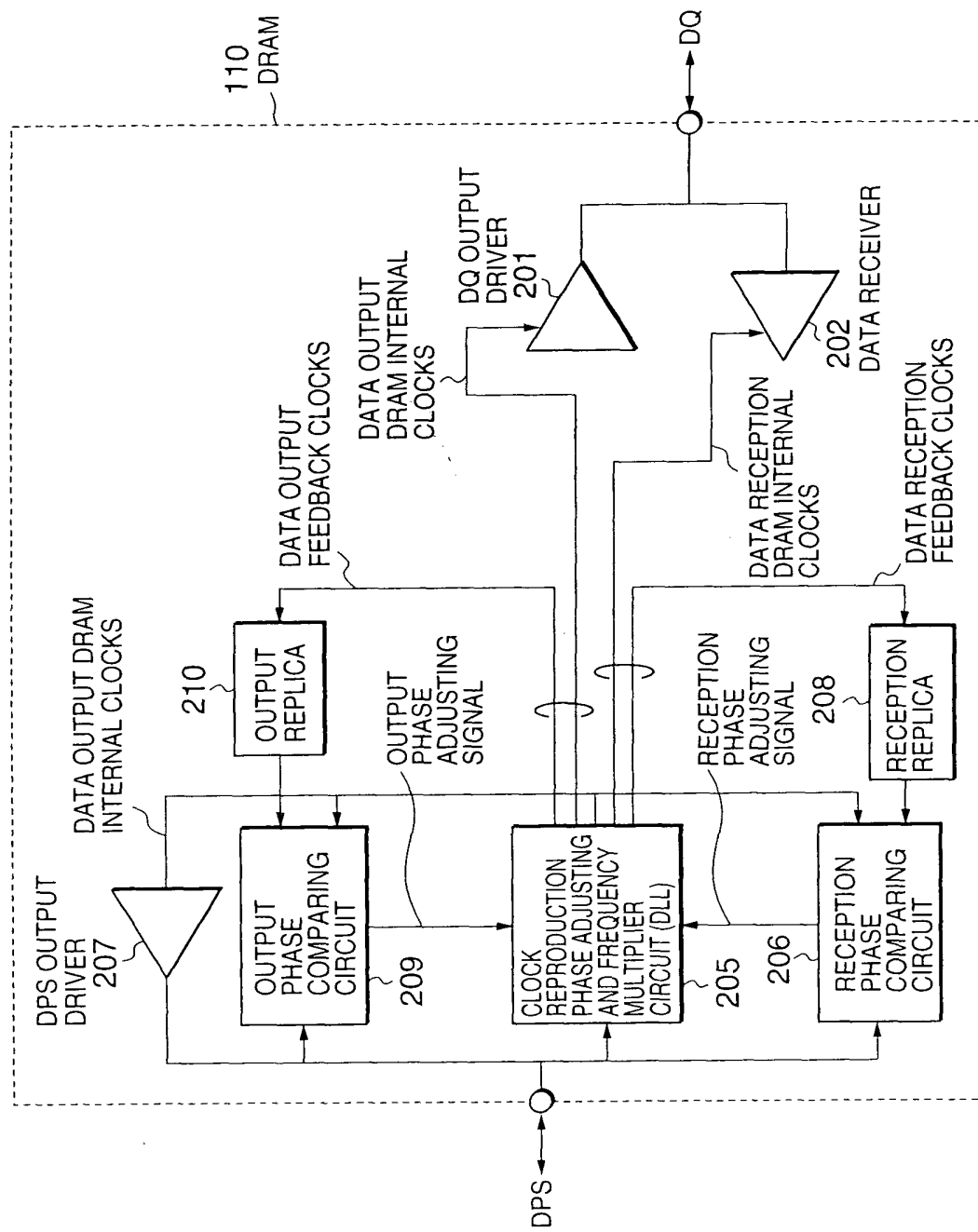


FIG. 23

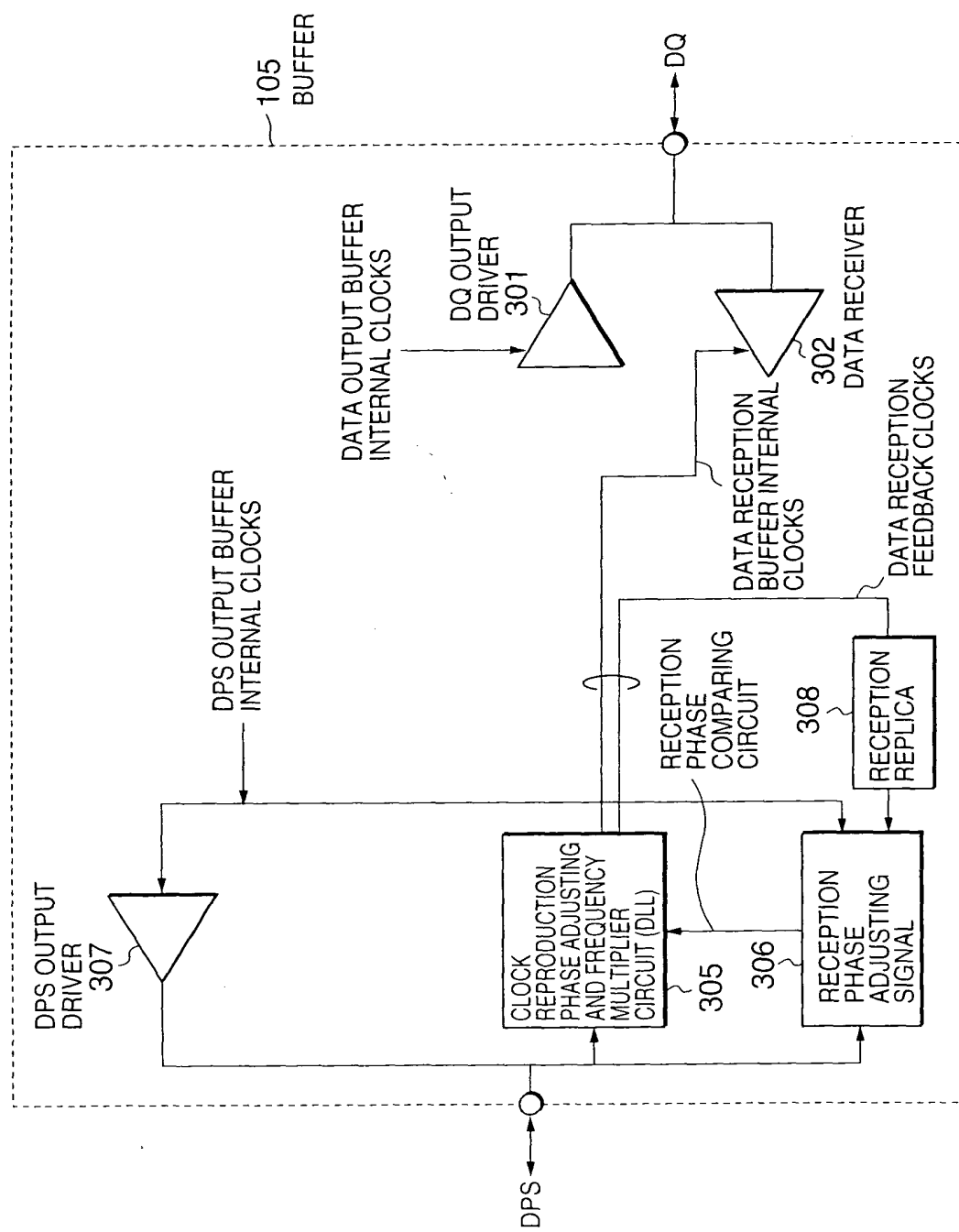


FIG. 24

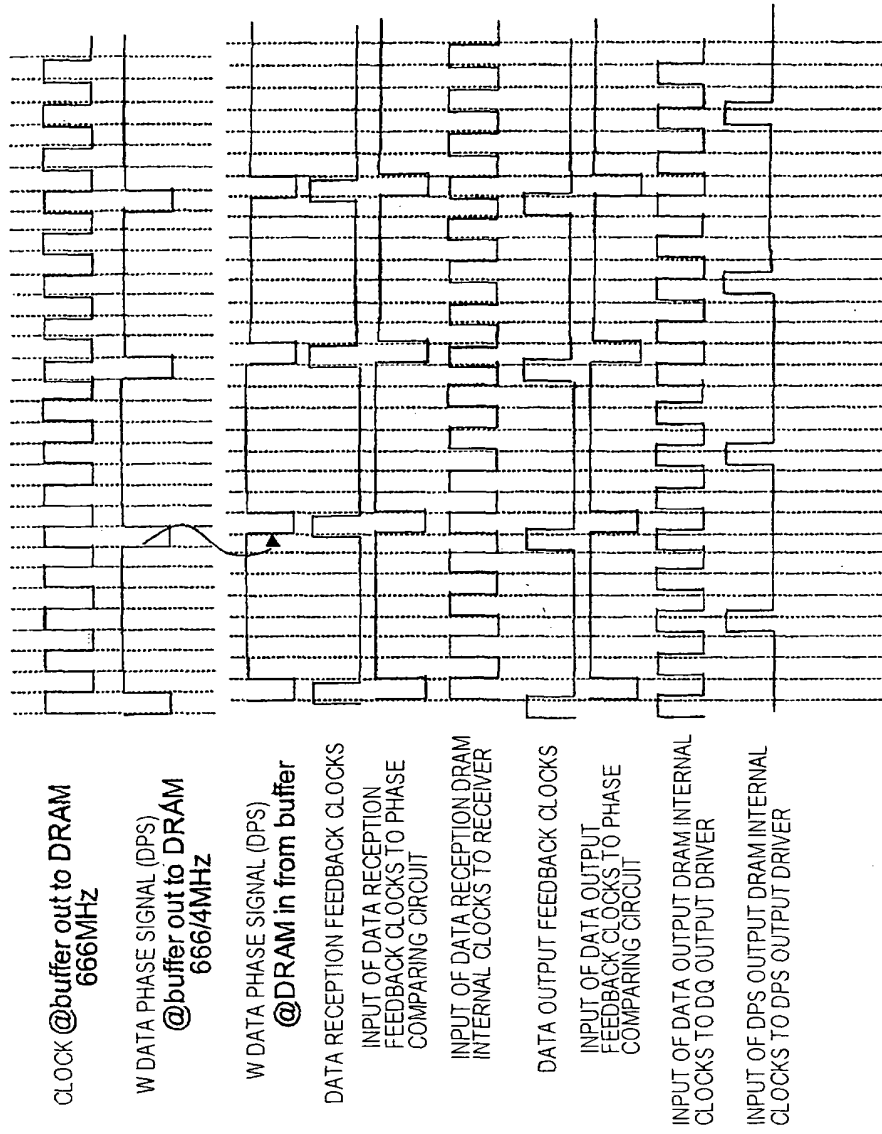


FIG. 25

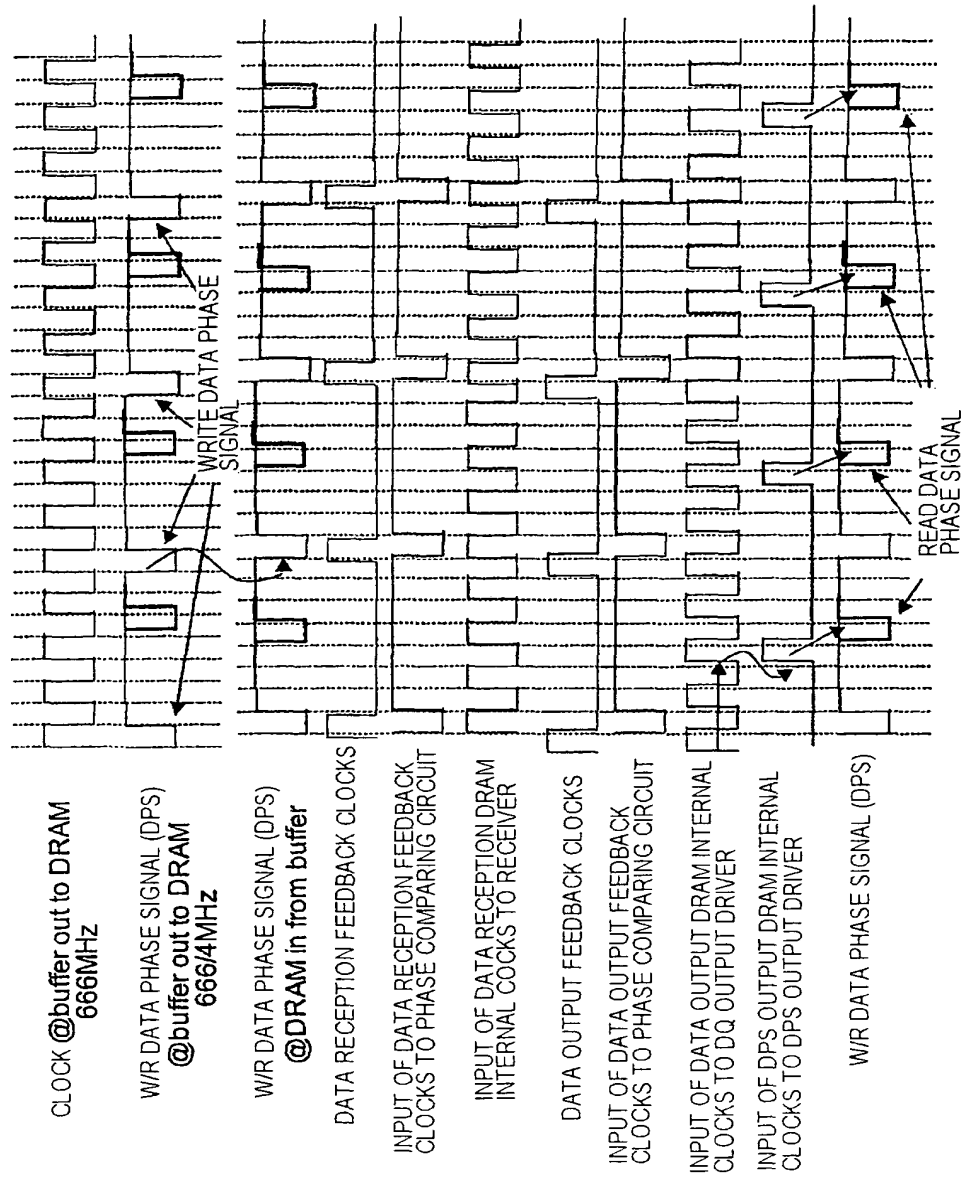


FIG. 26

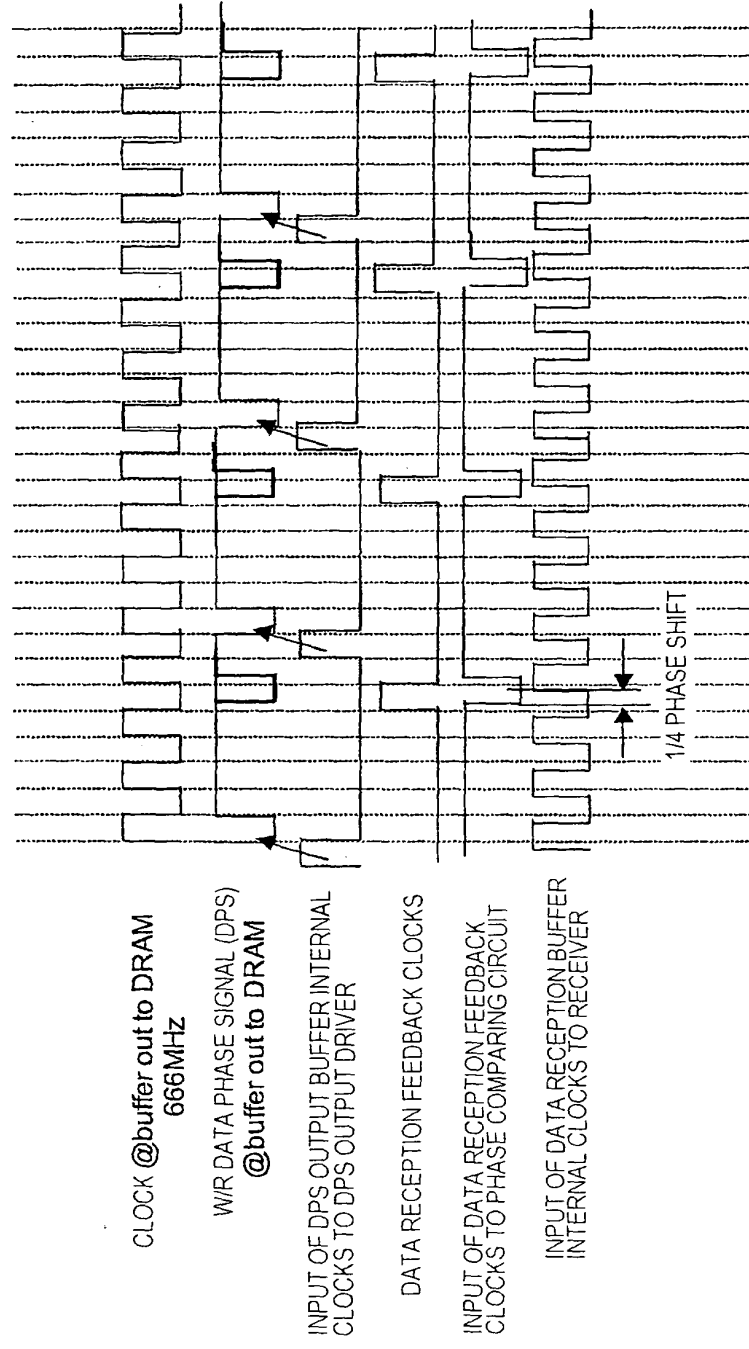


FIG. 27

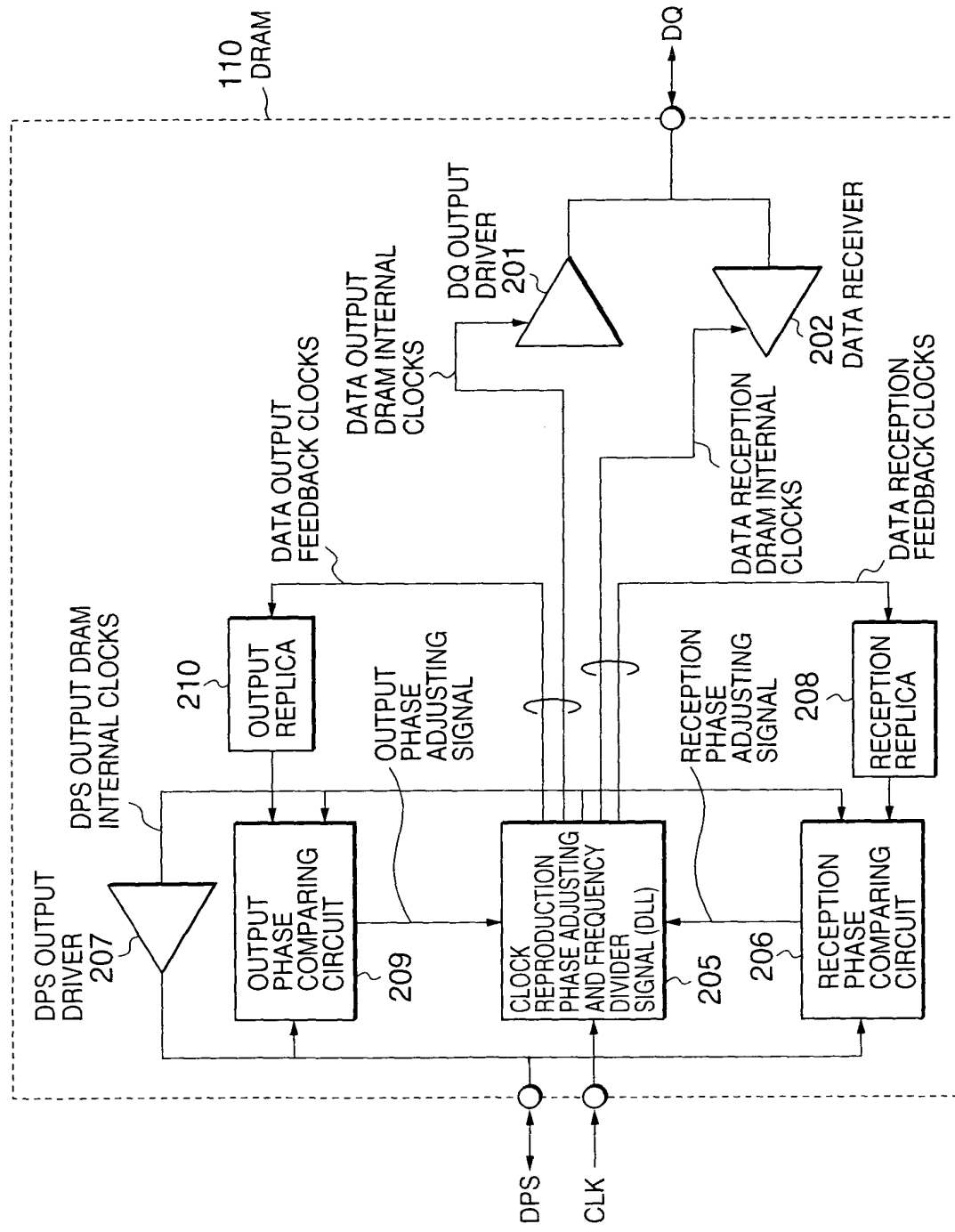


FIG.28

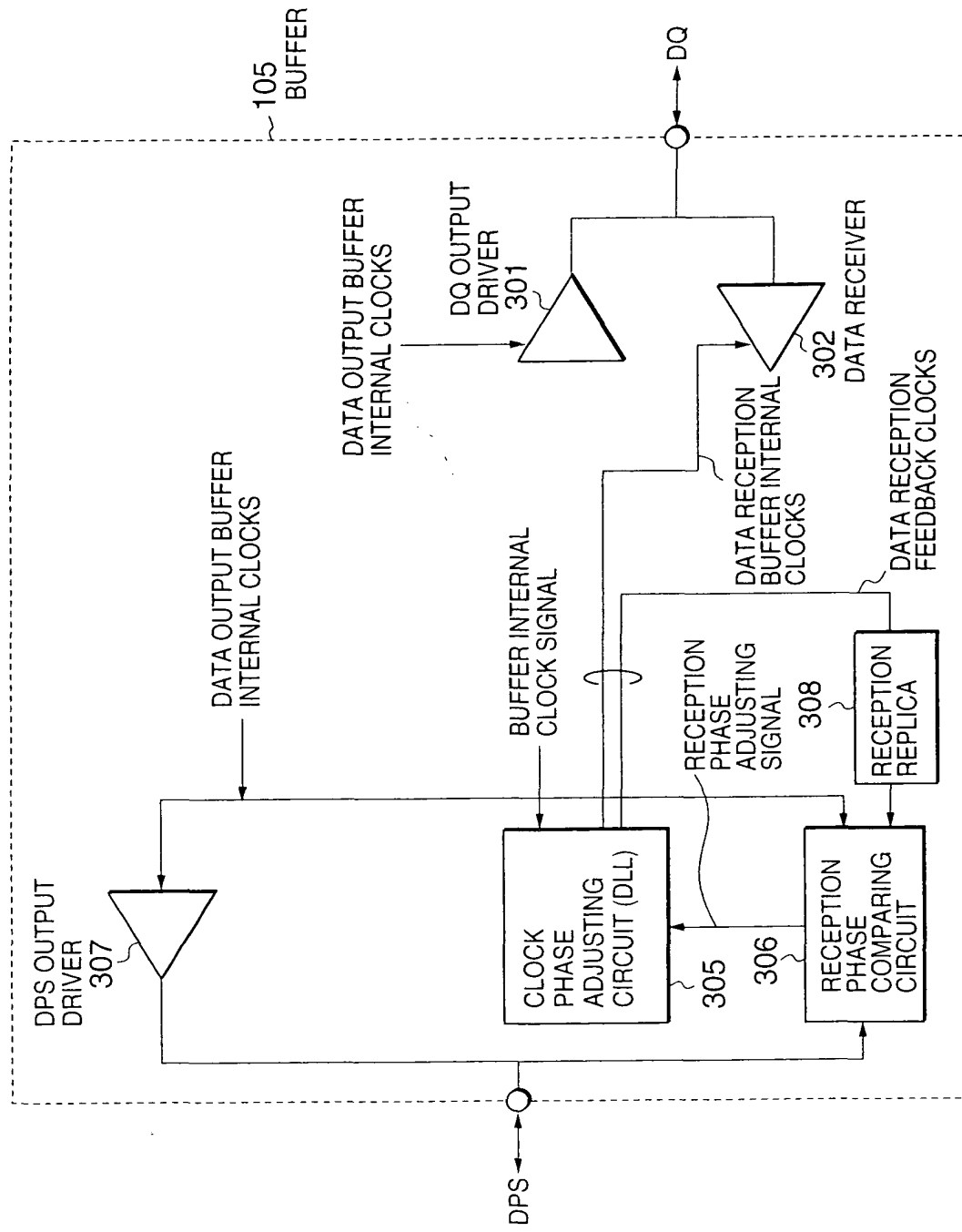


FIG.29

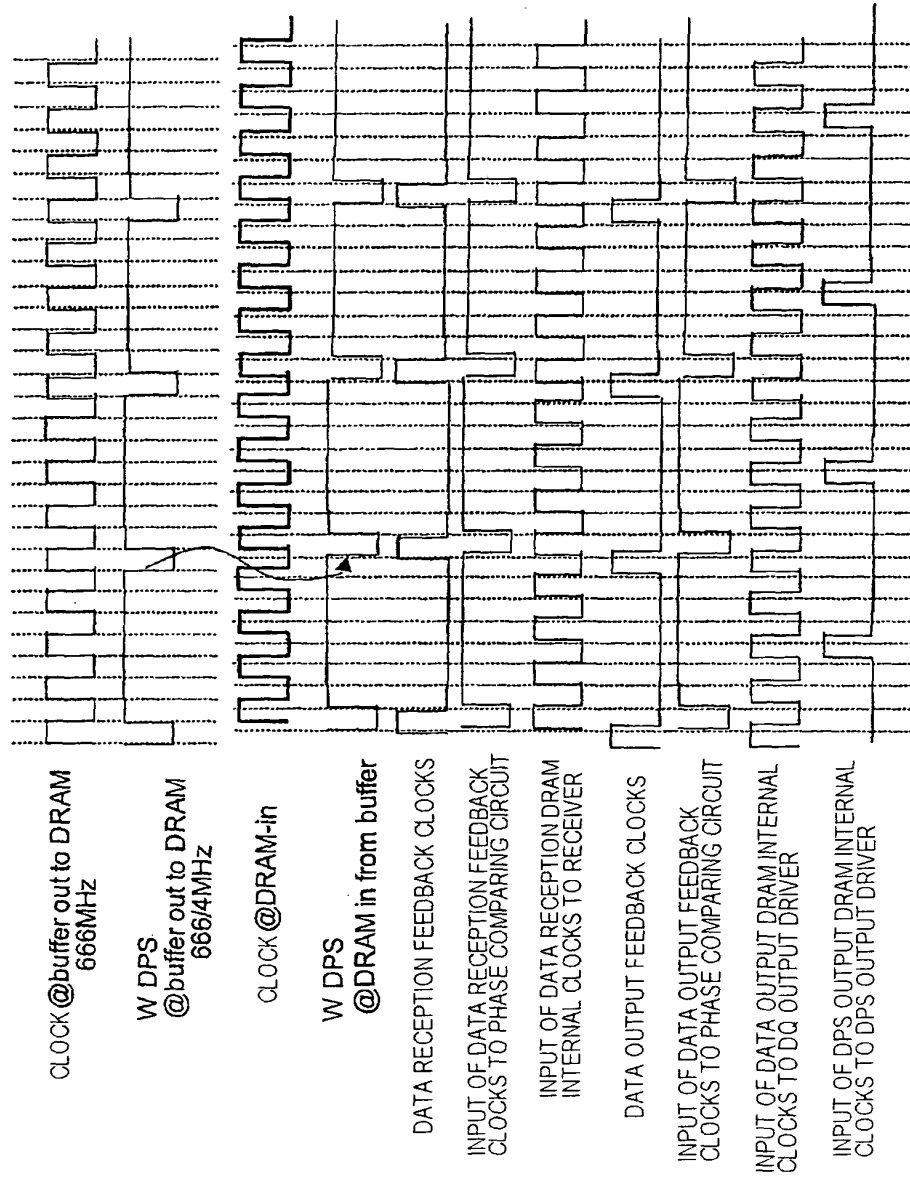


FIG. 30

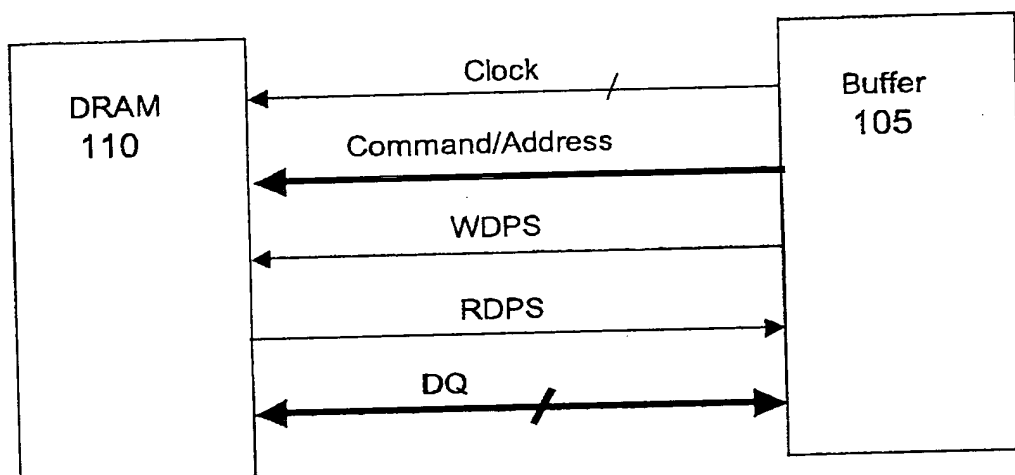


FIG. 31

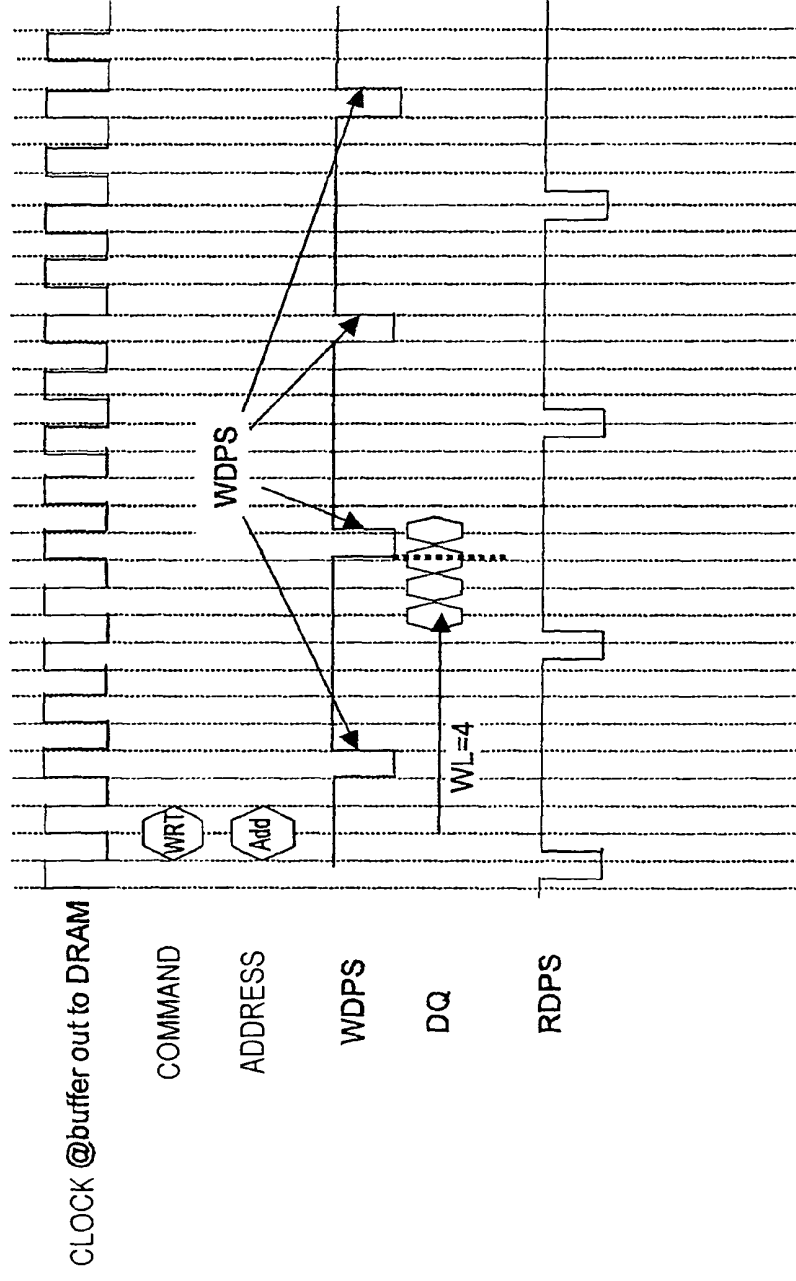


FIG. 32

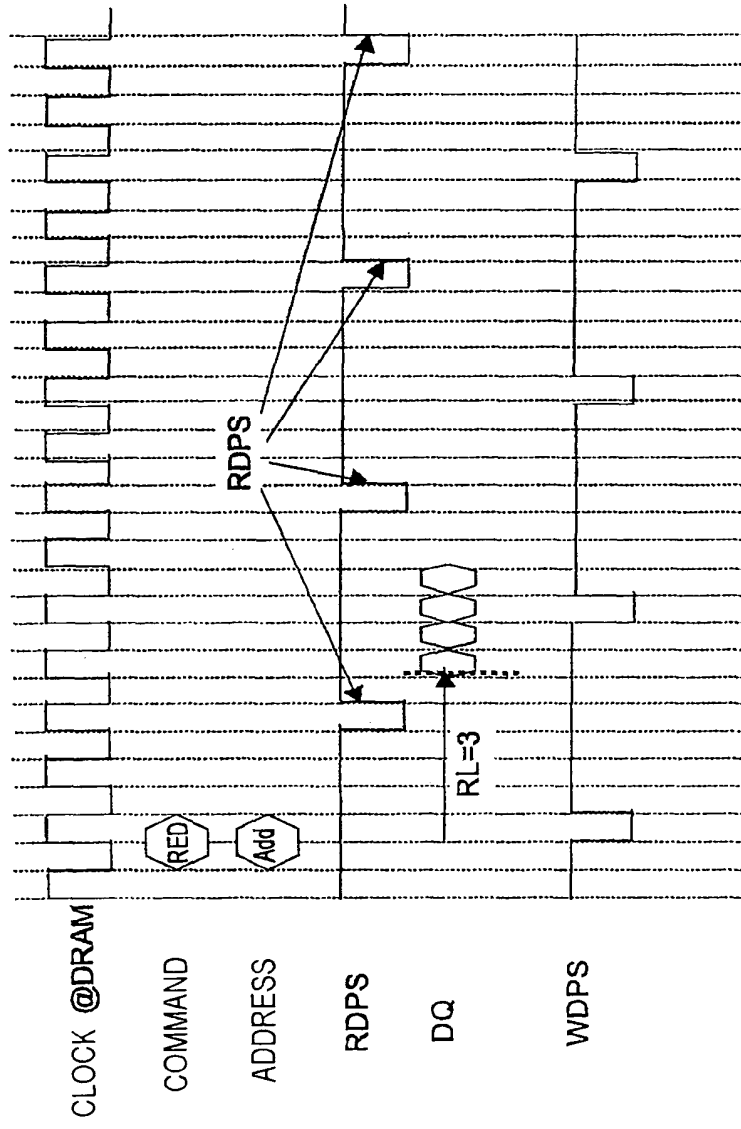


FIG. 33

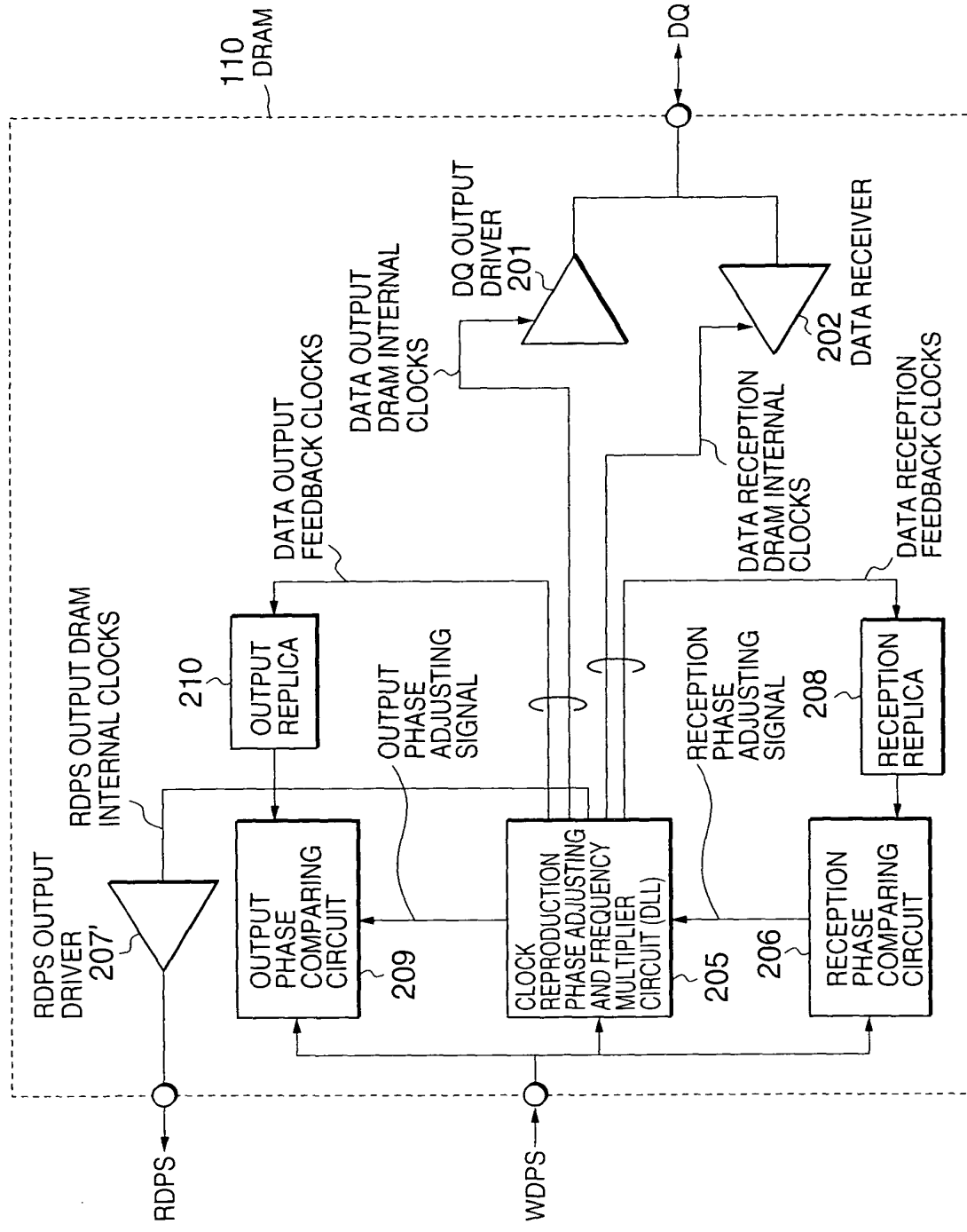


FIG. 34

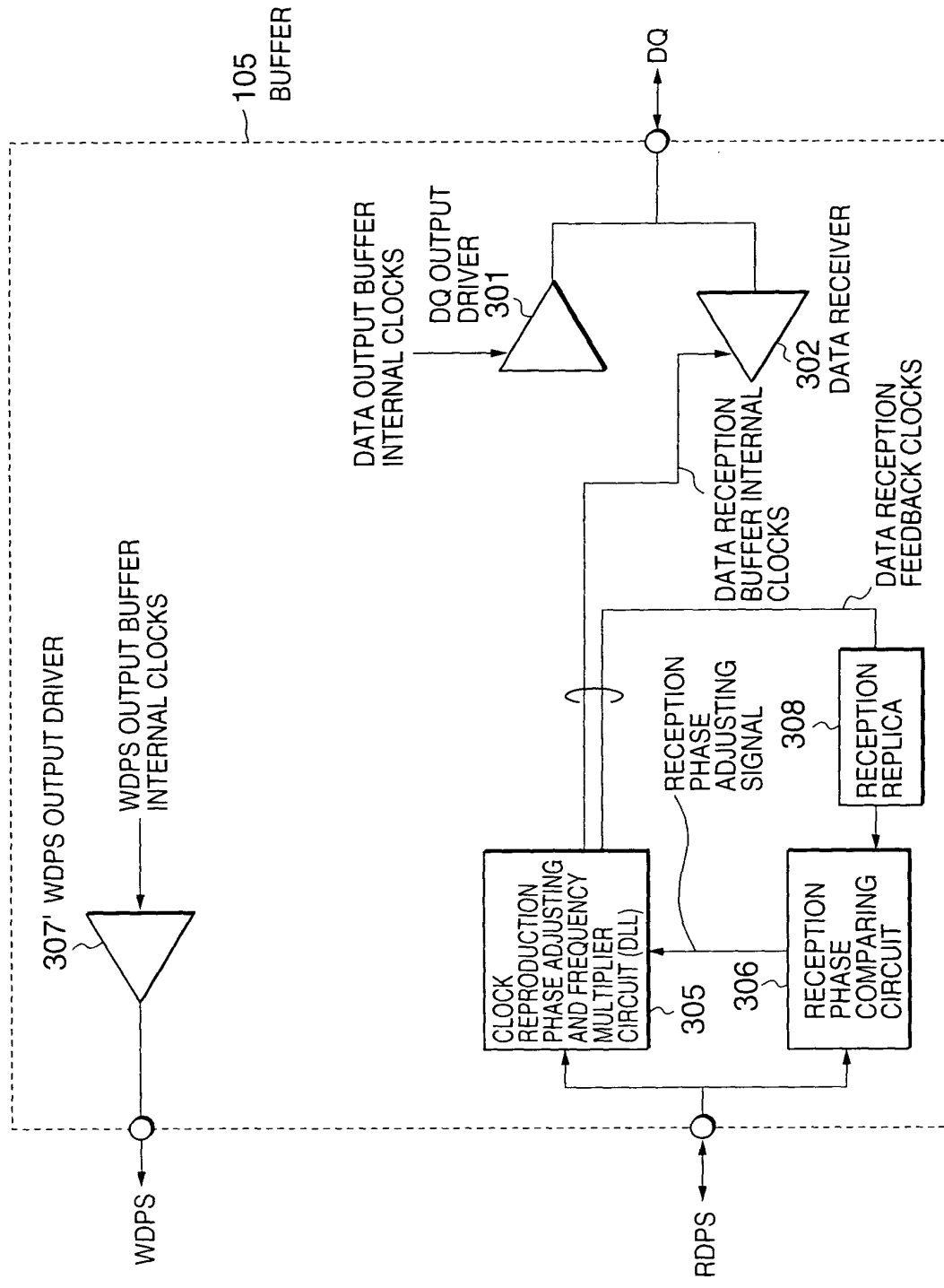


FIG.35

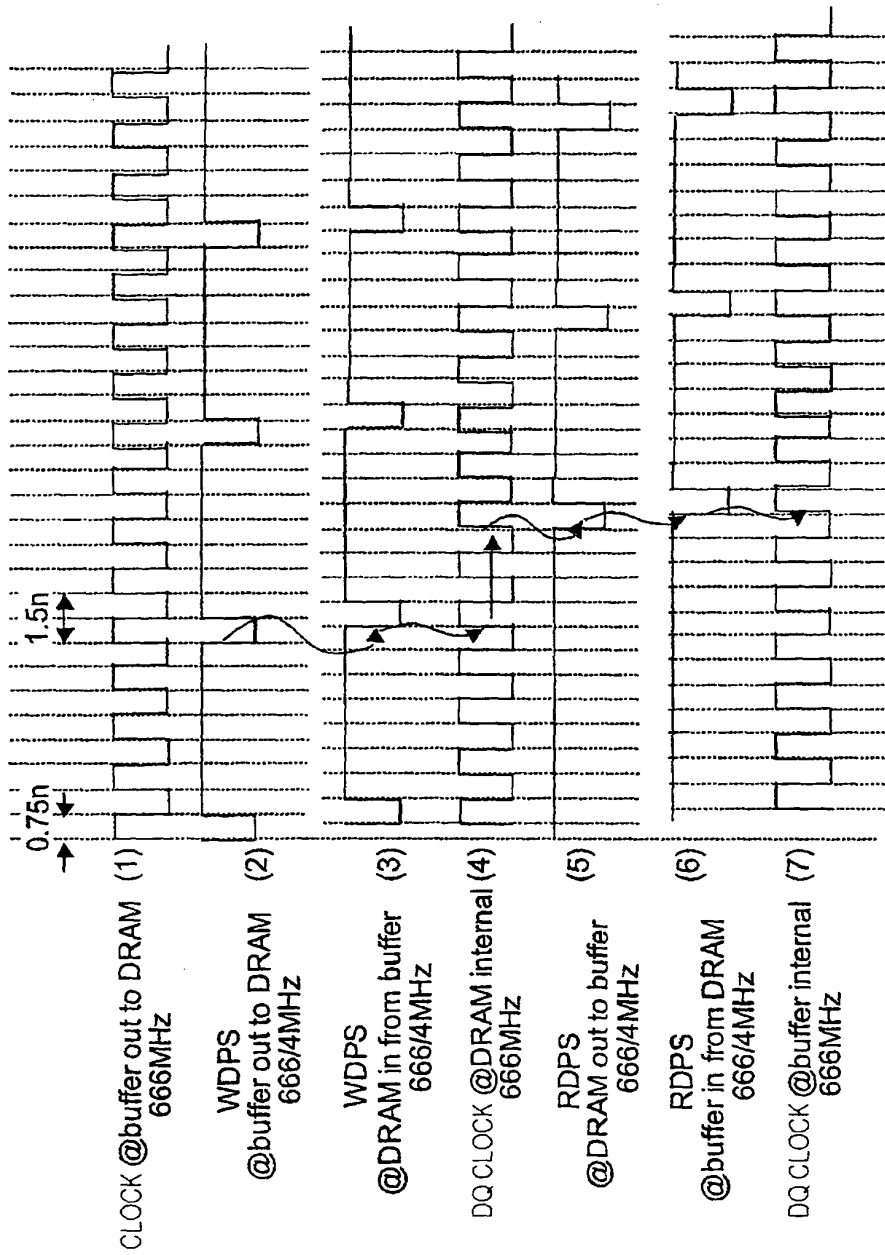


FIG. 36

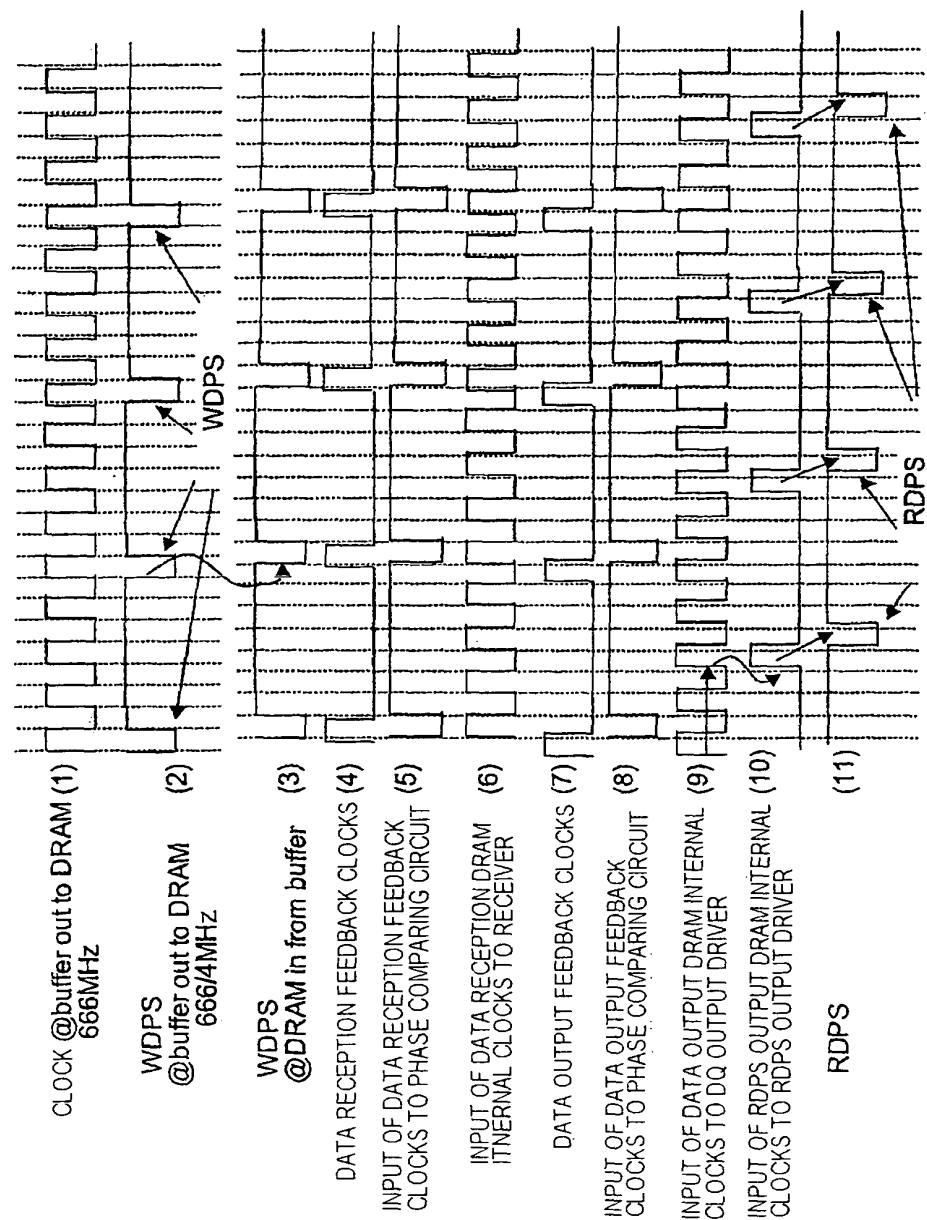


FIG. 37

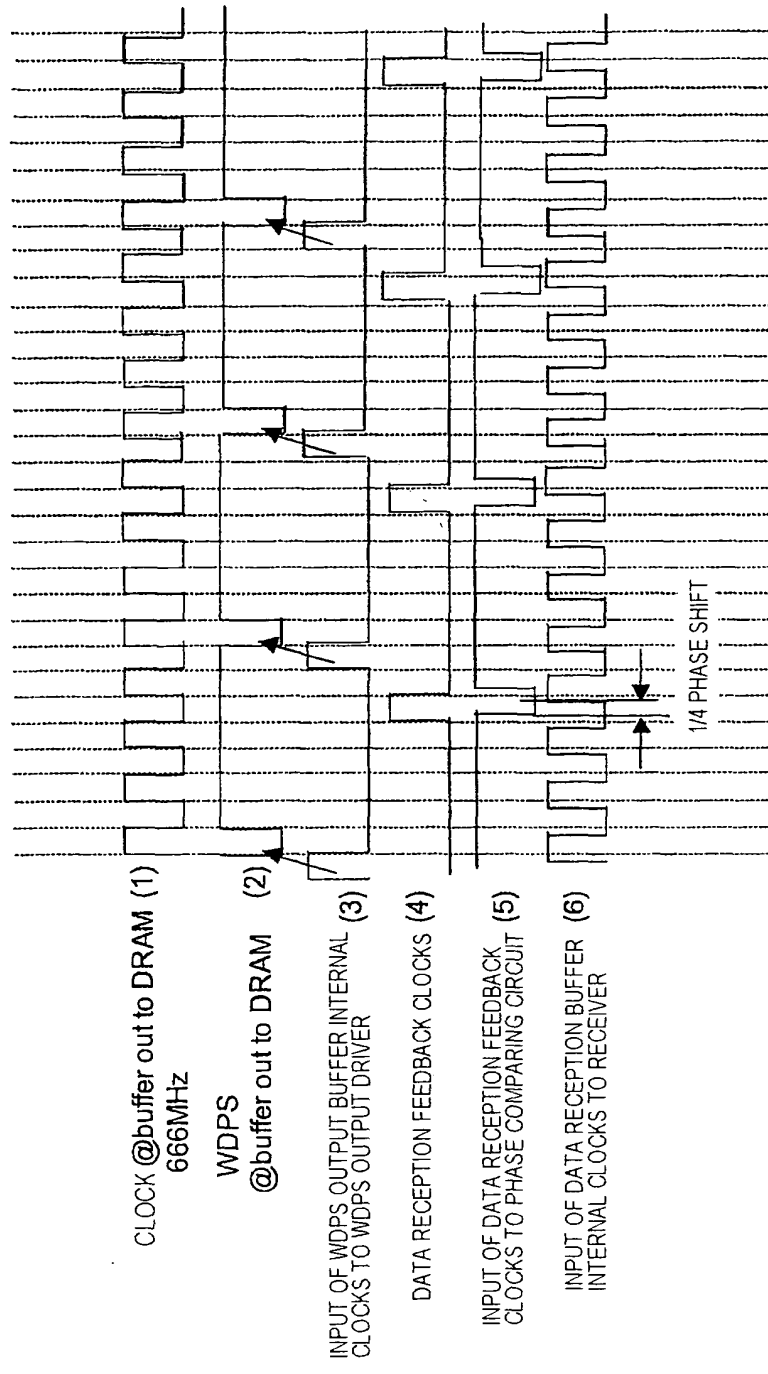


FIG. 38

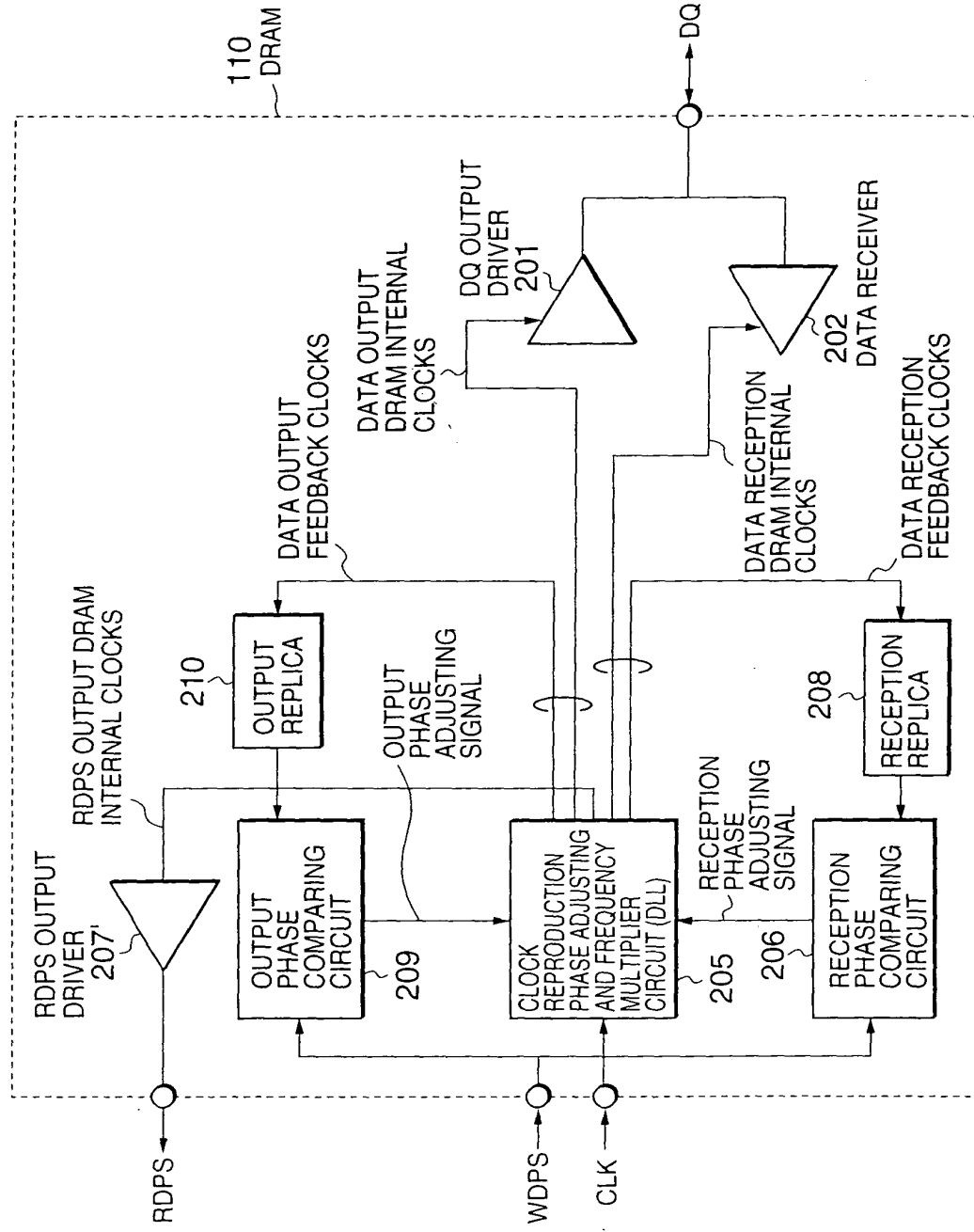


FIG.39

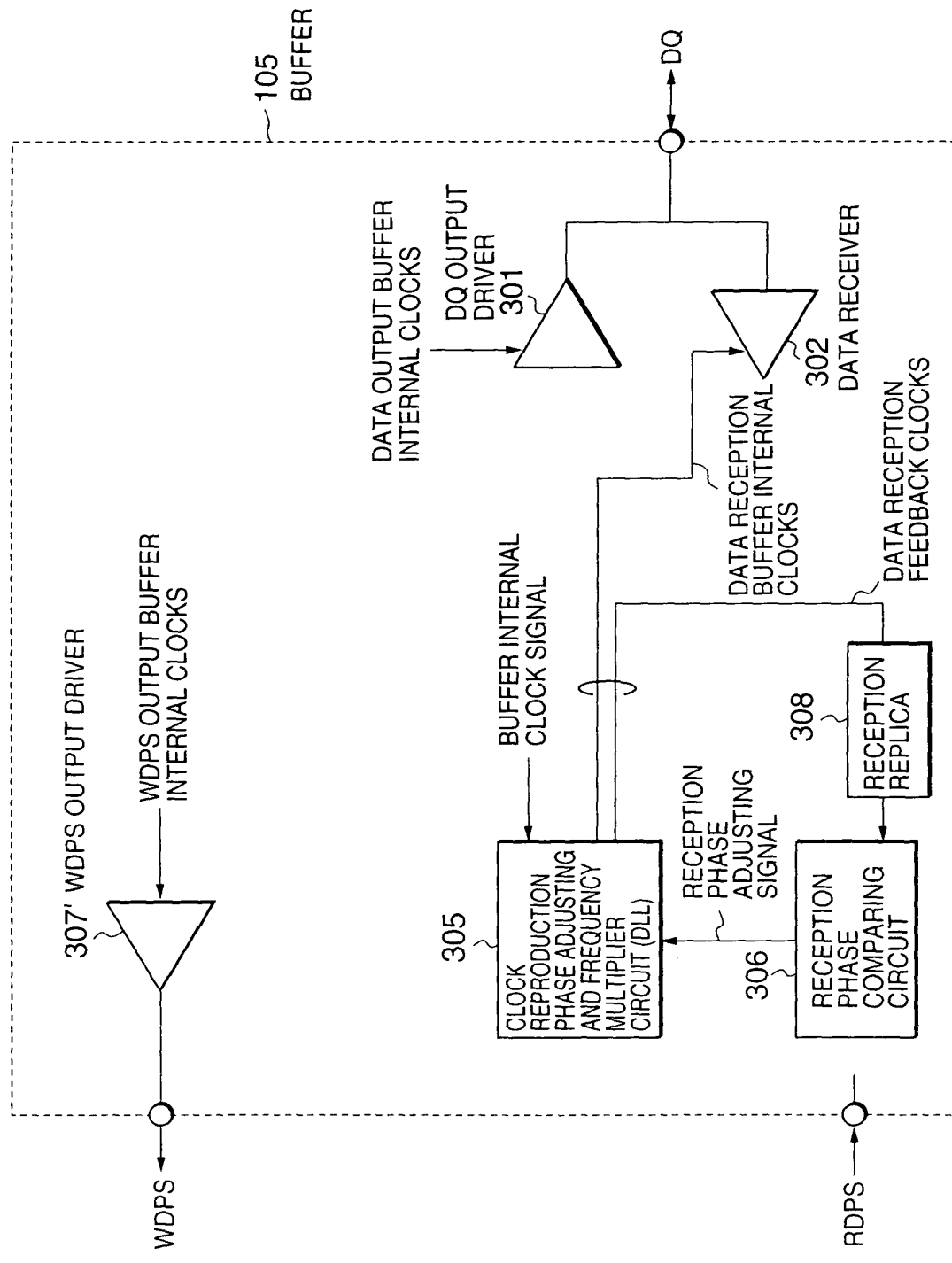


FIG.40

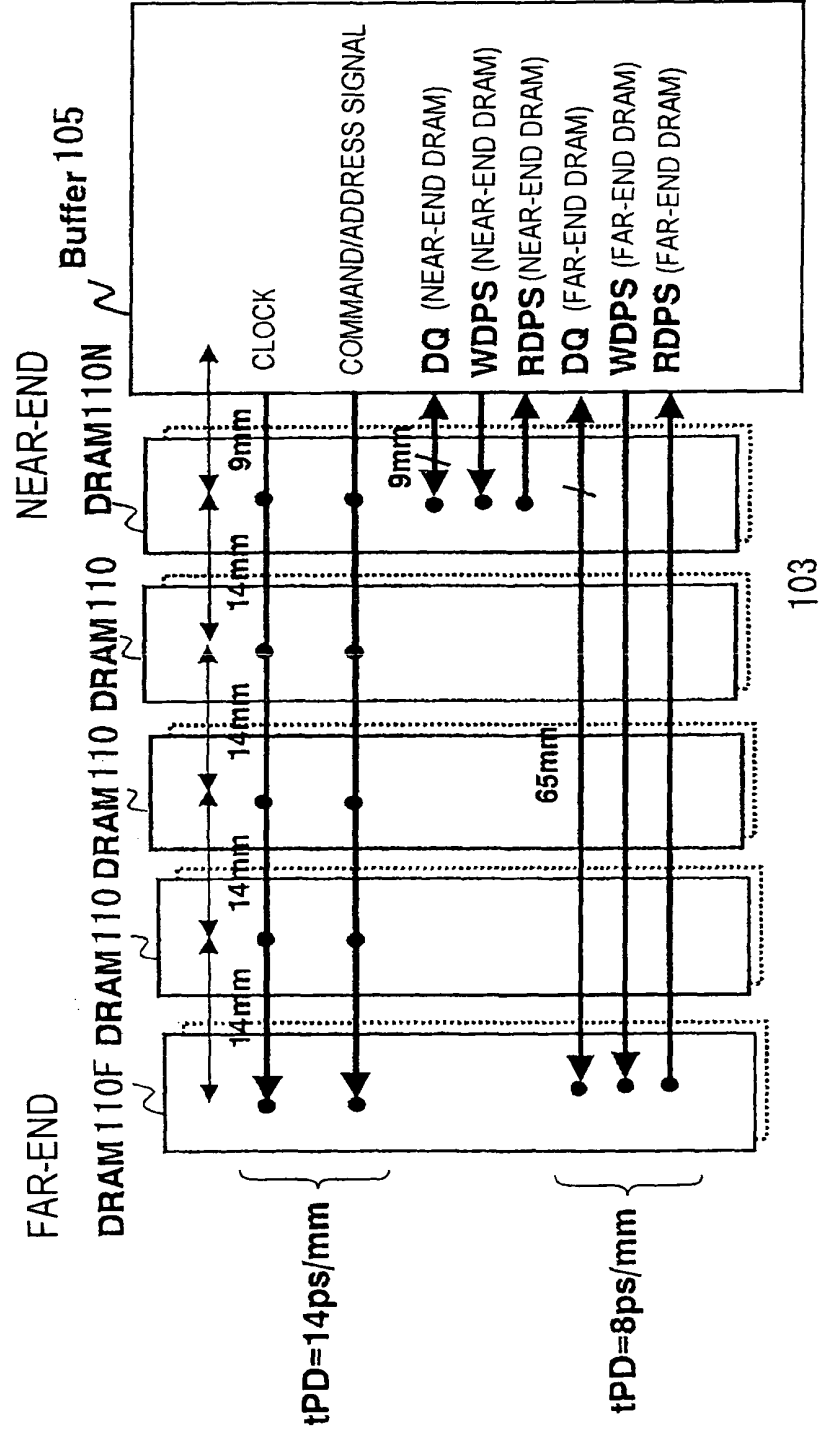


FIG. 41

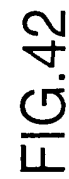


FIG. 42

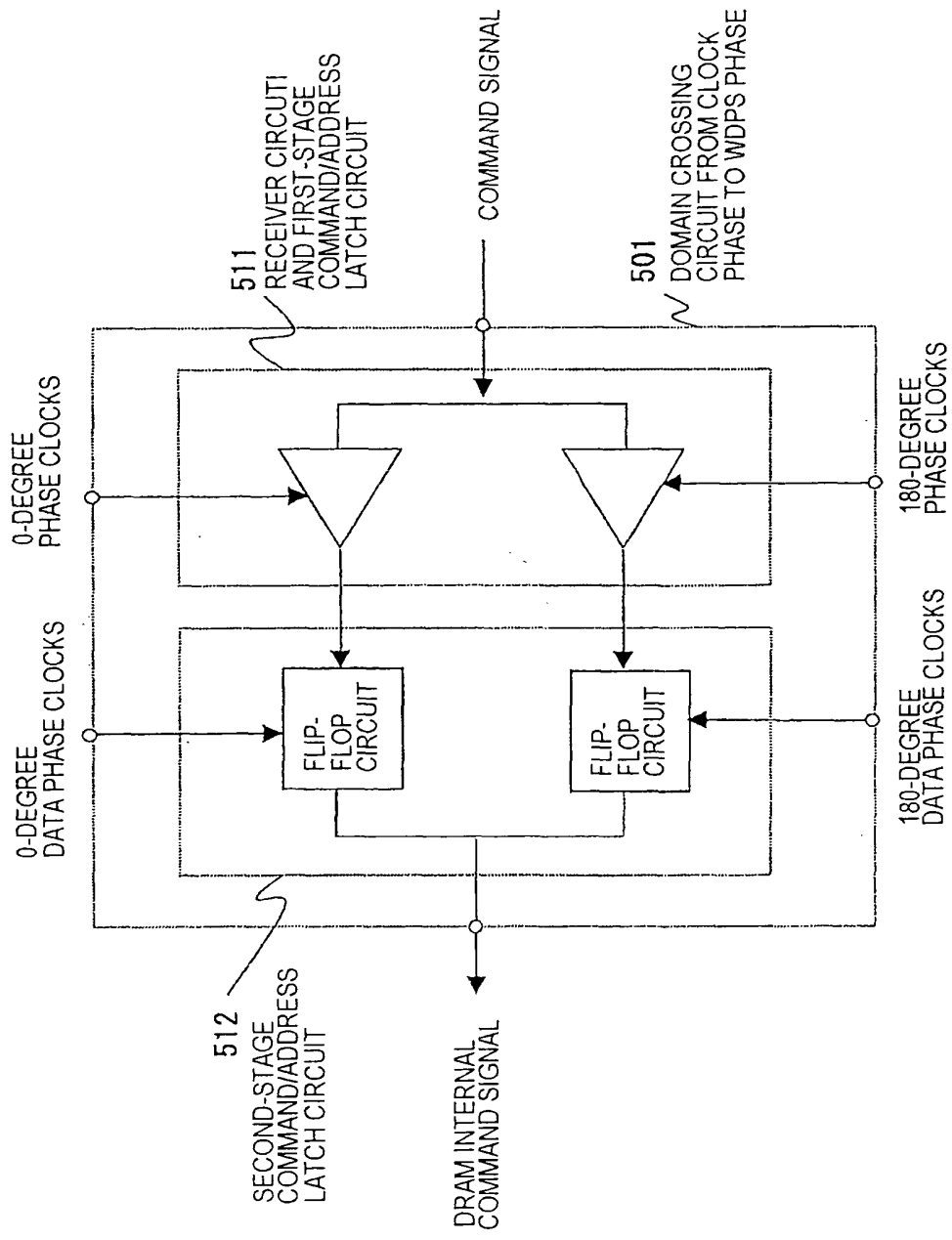


FIG. 43

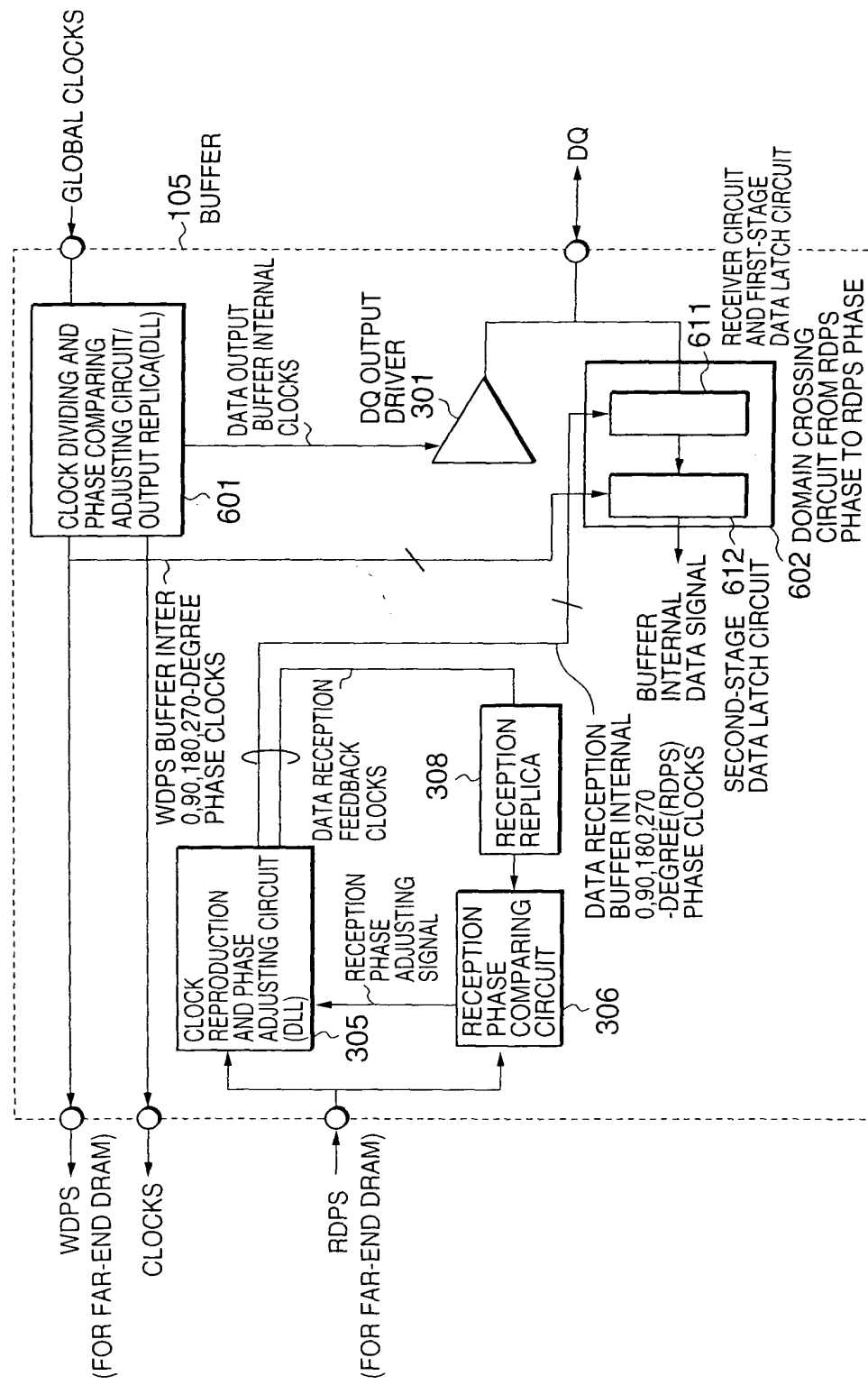


FIG. 44

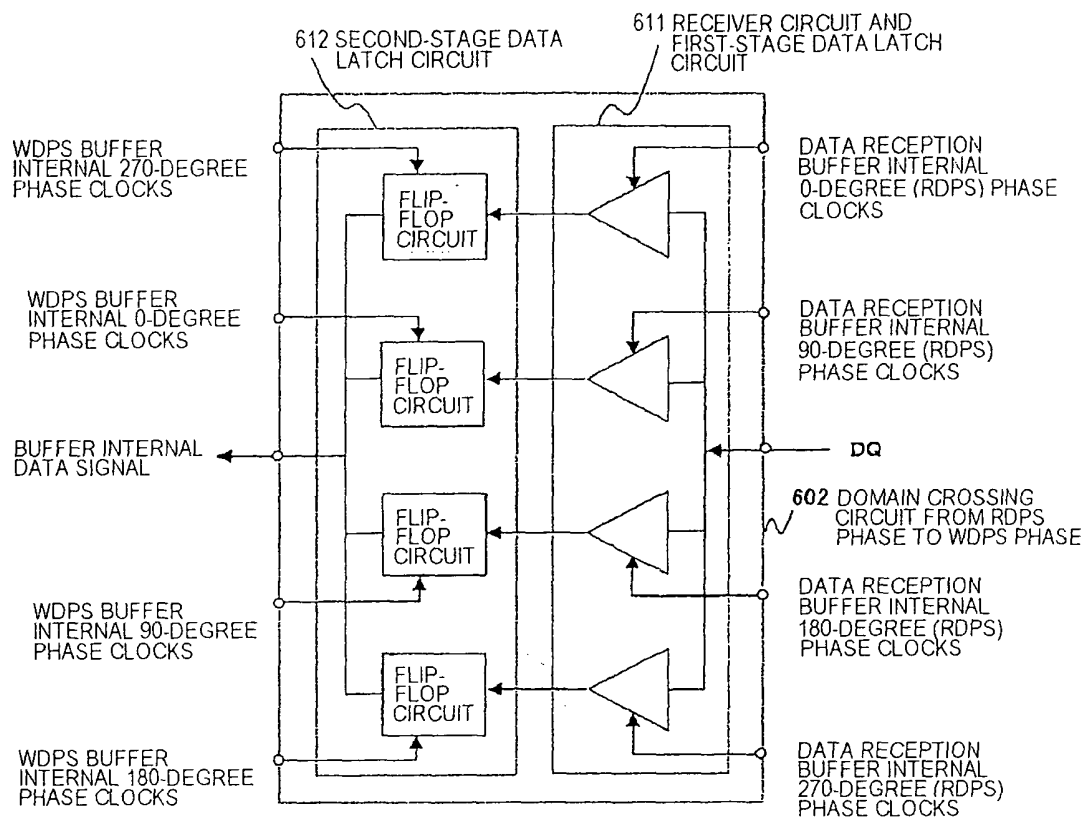


FIG. 45

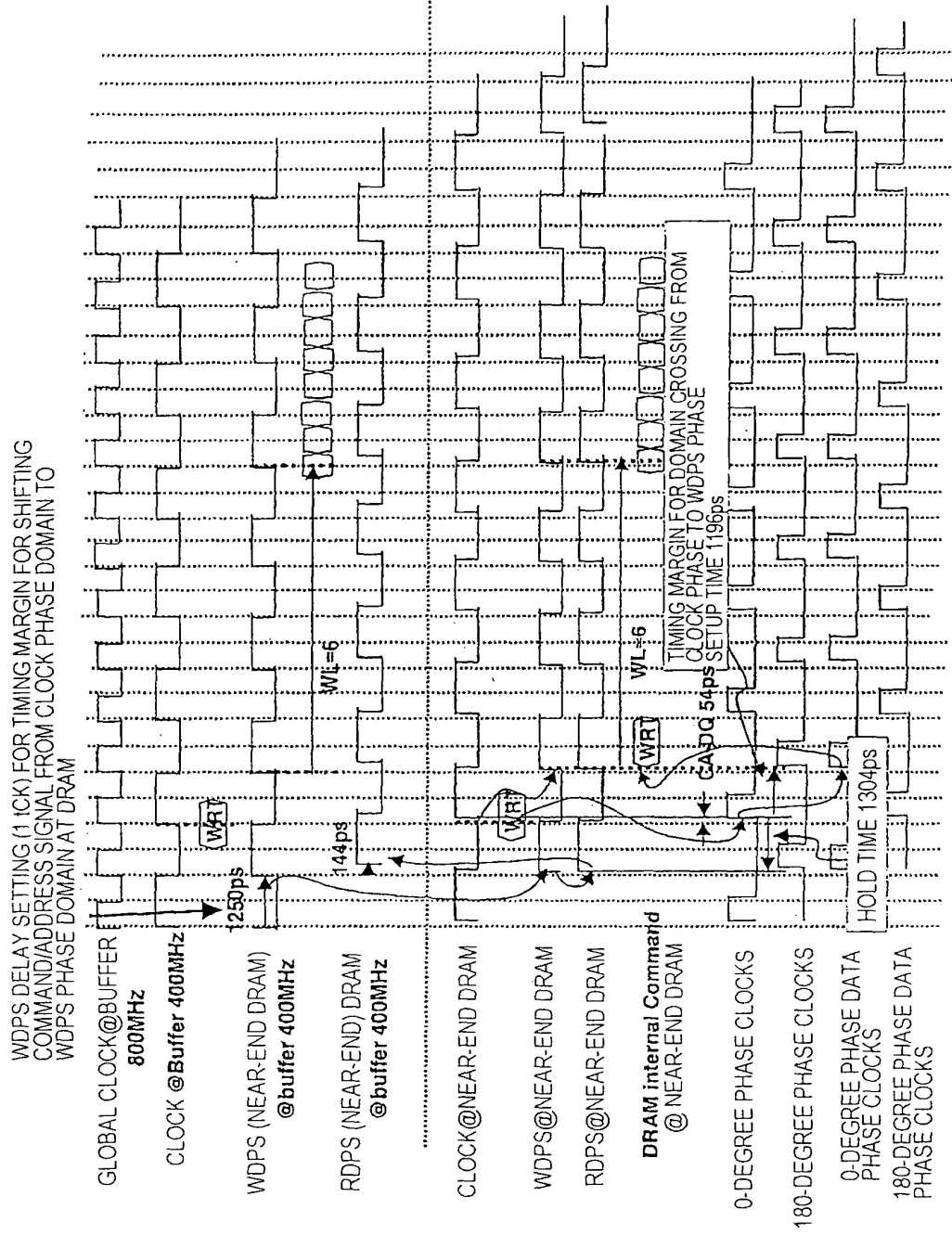


FIG. 46

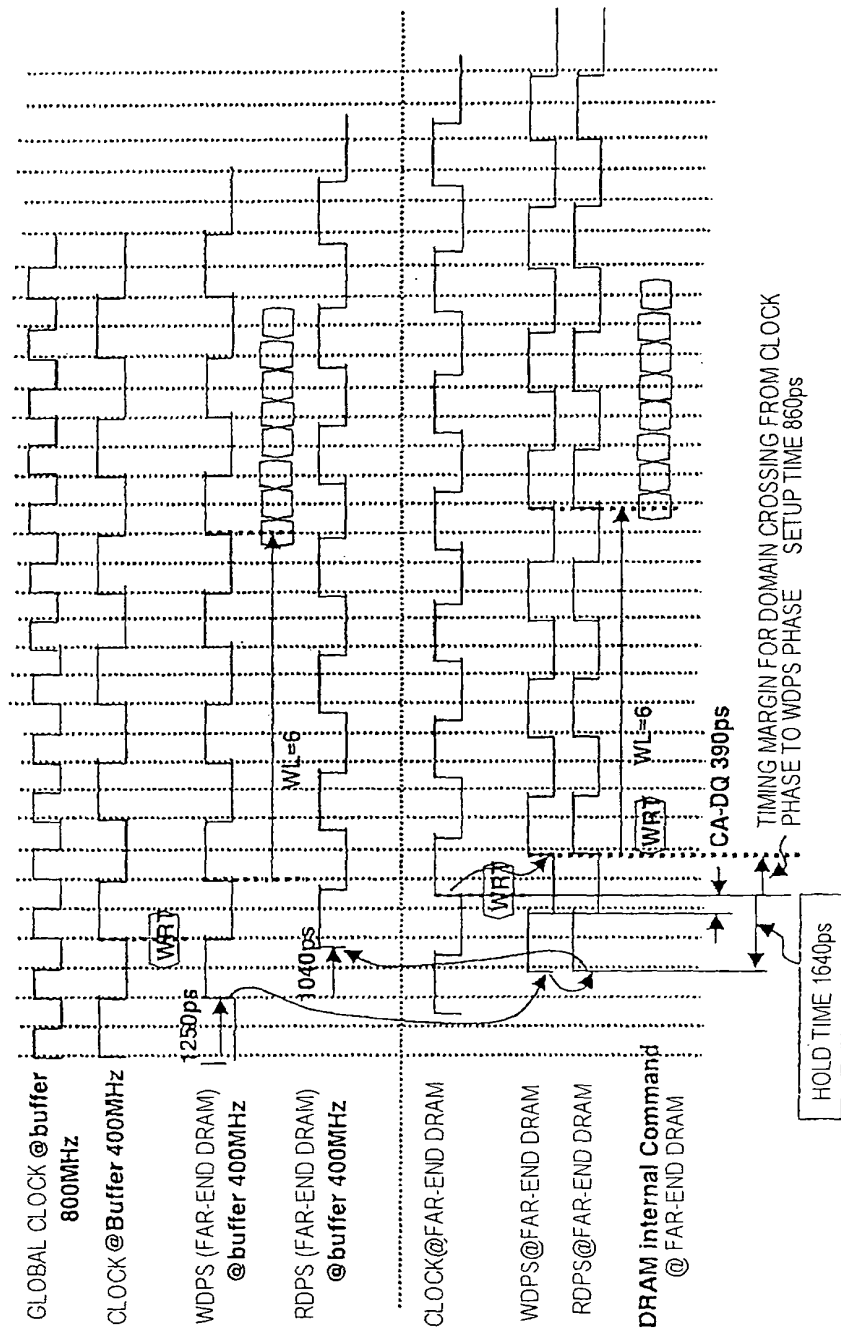


FIG. 47

WDPS DELAY SETTING (11CK) FOR TIMING MARGIN FOR SHIFTING
 COMMAND/ADDRESS SIGNAL FROM CLOCK PHASE DOMAIN TO WDPS PHASE
 DOMAIN AT DRAM

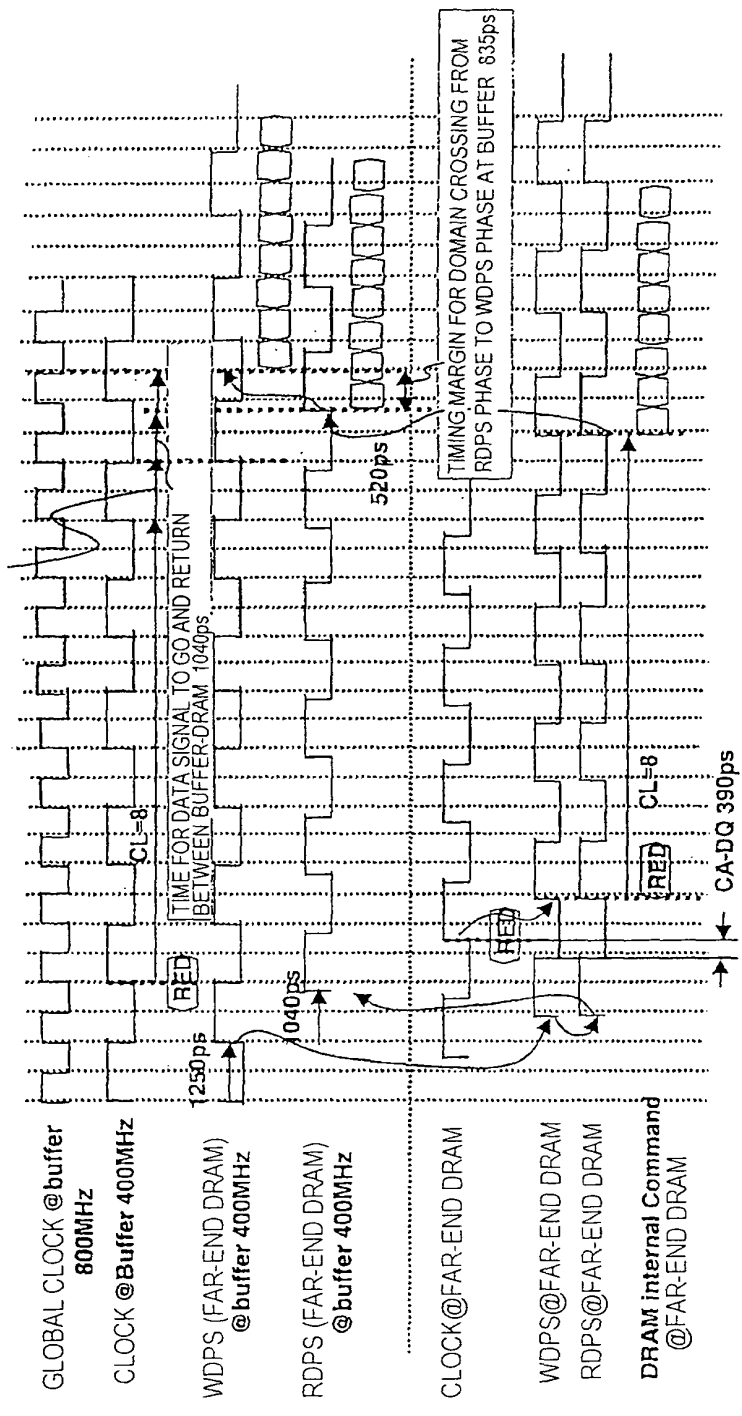


FIG. 48

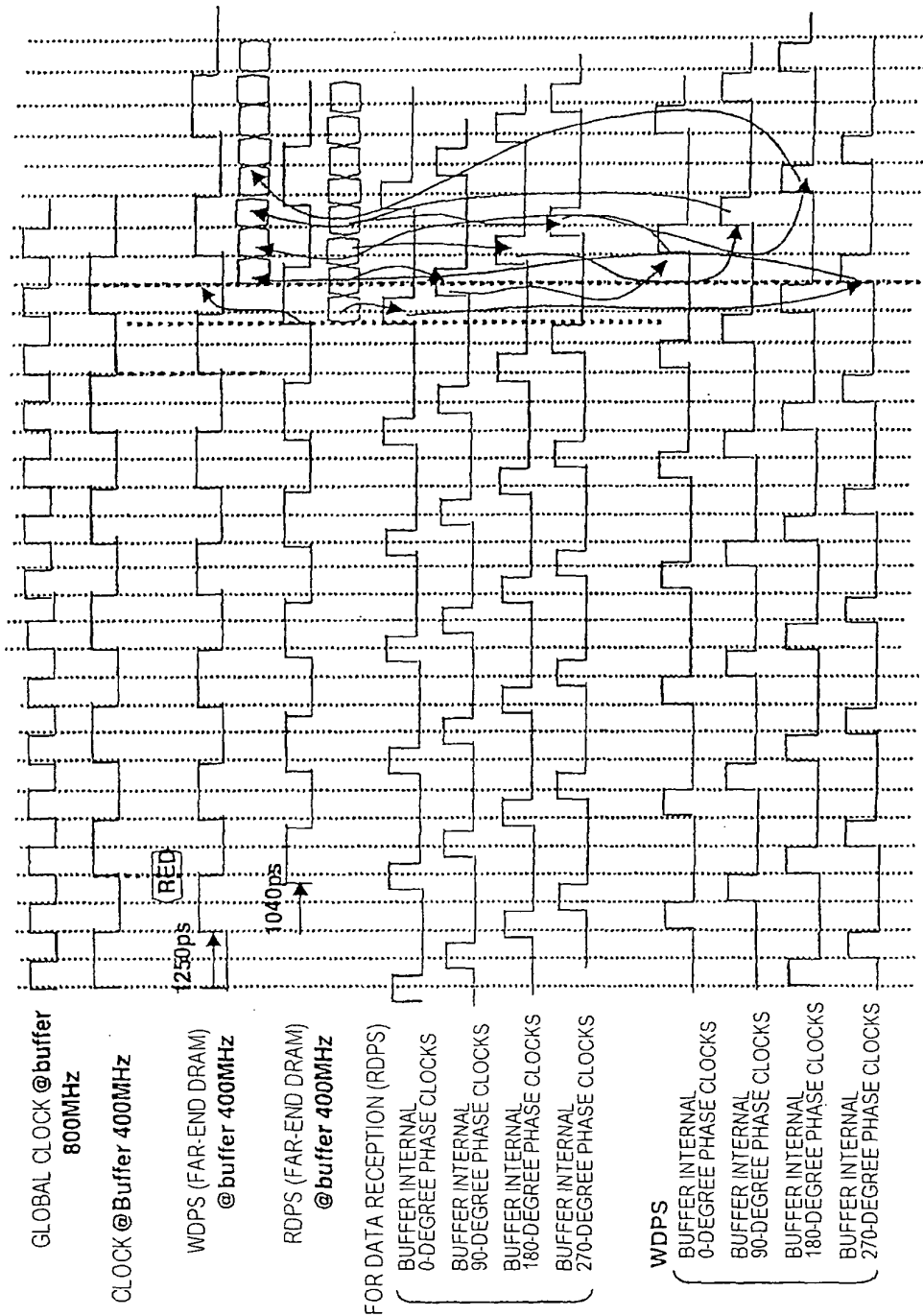


FIG. 49

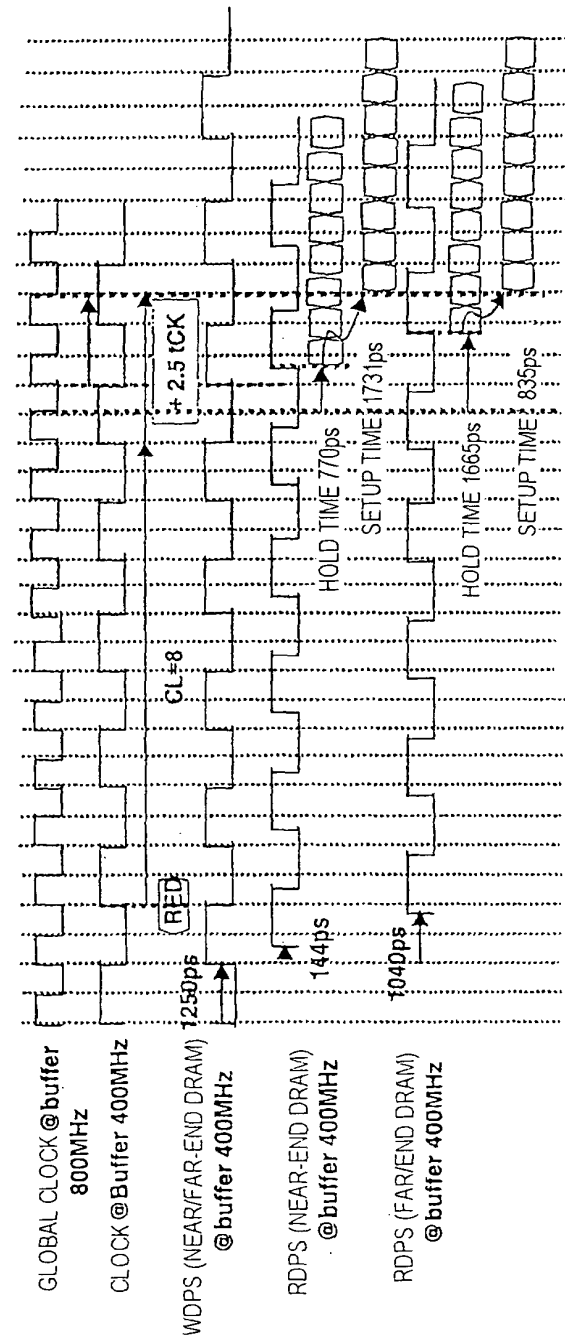


FIG. 50

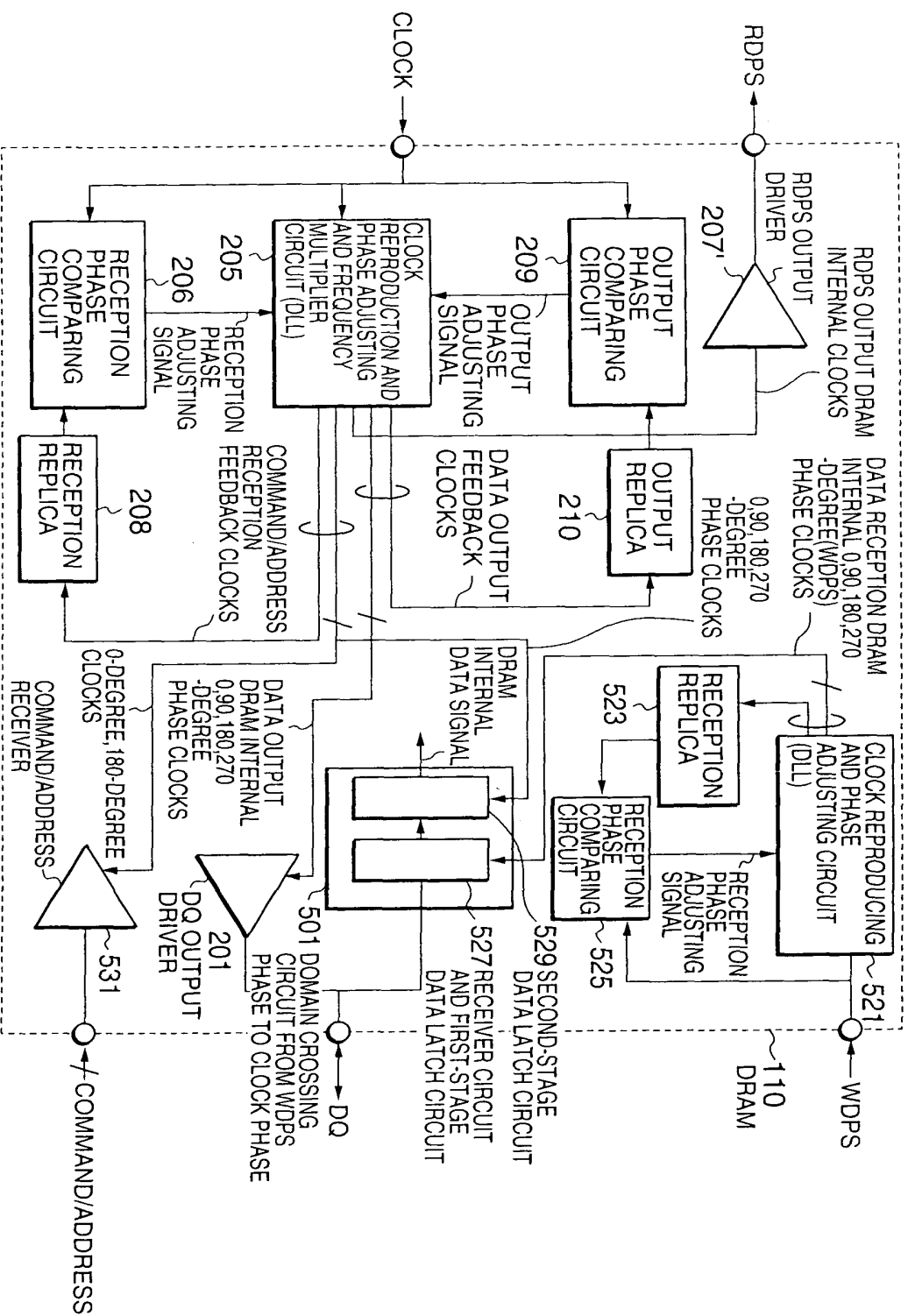


FIG. 51

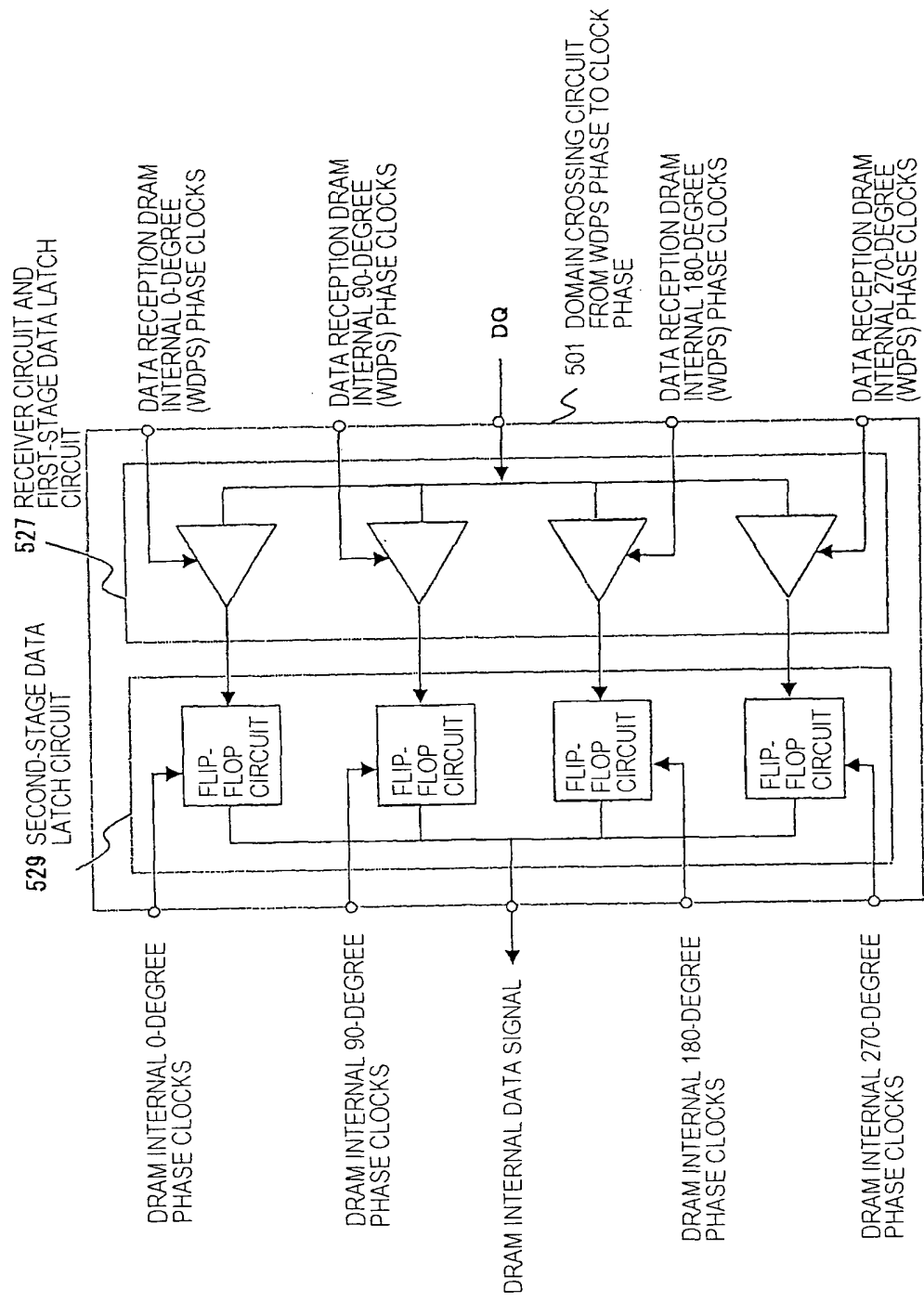


FIG. 52

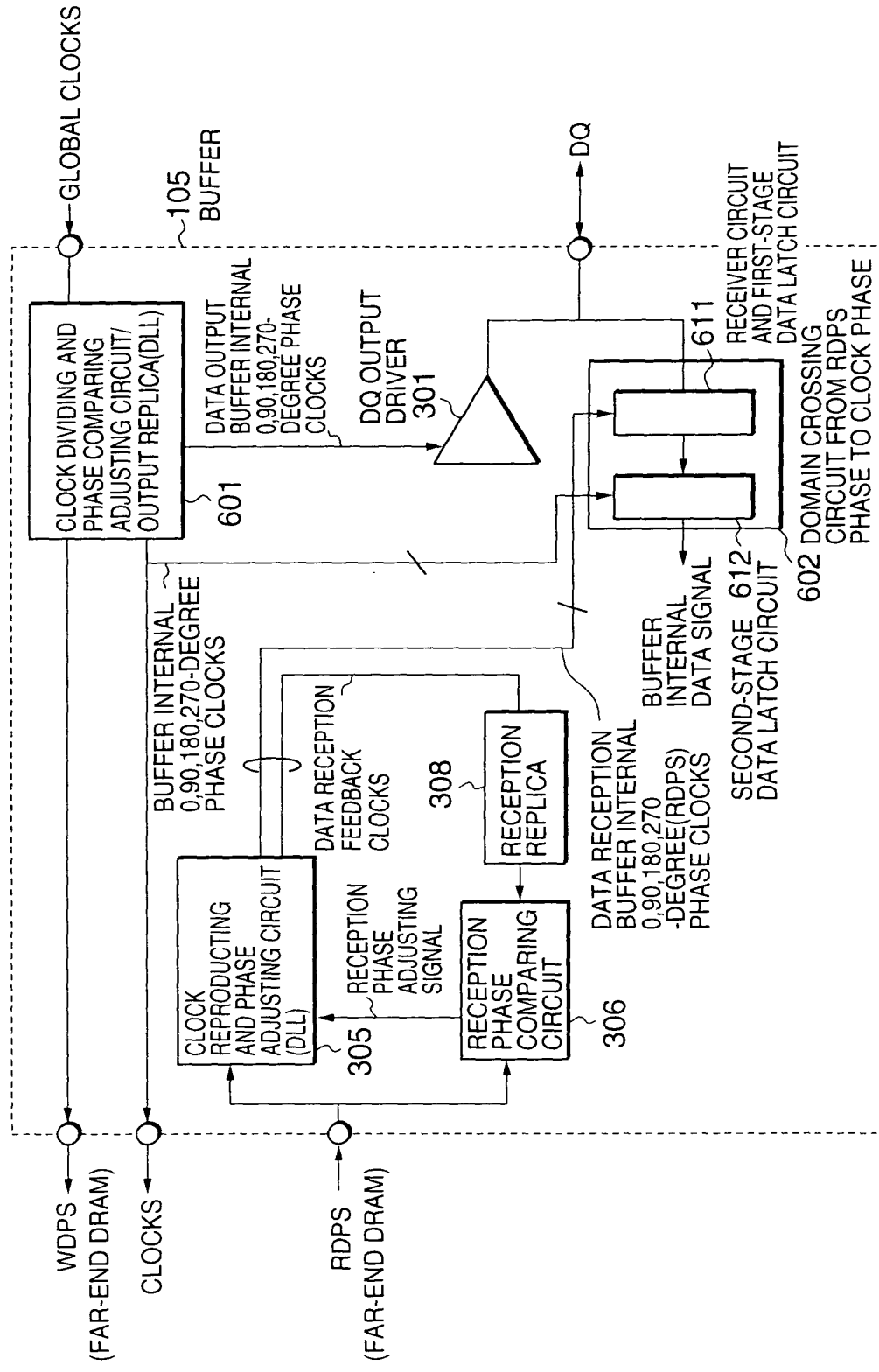


FIG.53

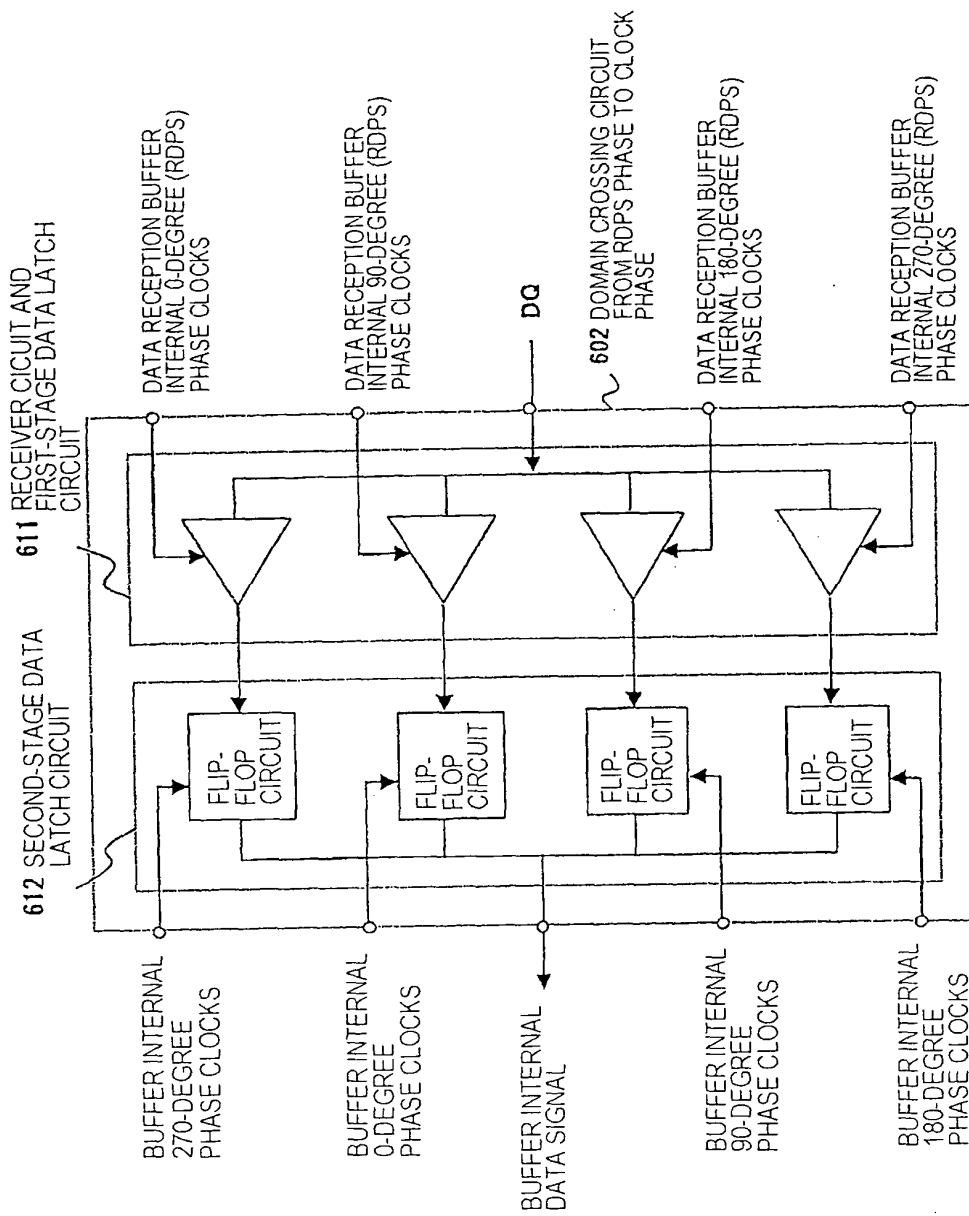


FIG. 54

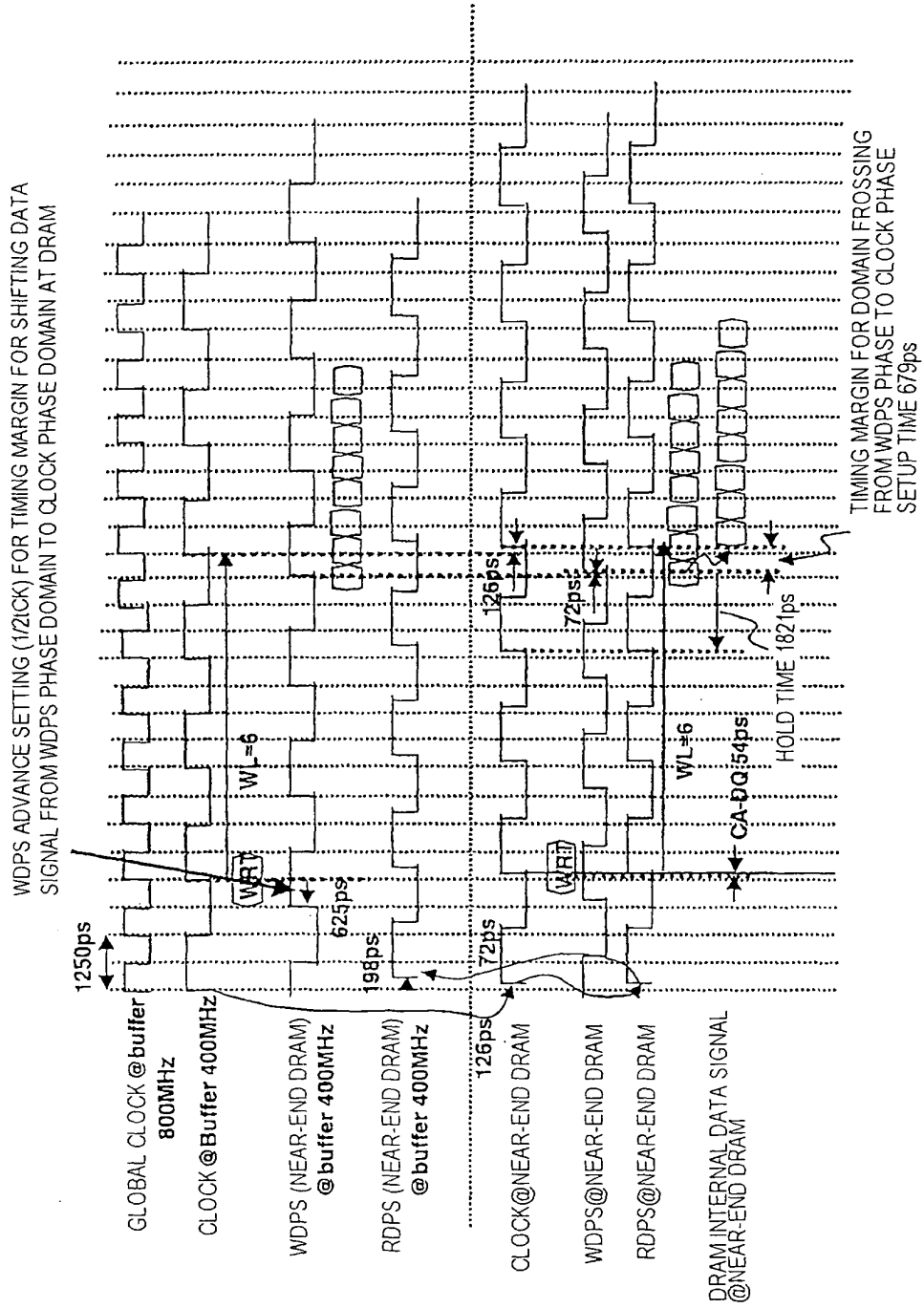


FIG. 55

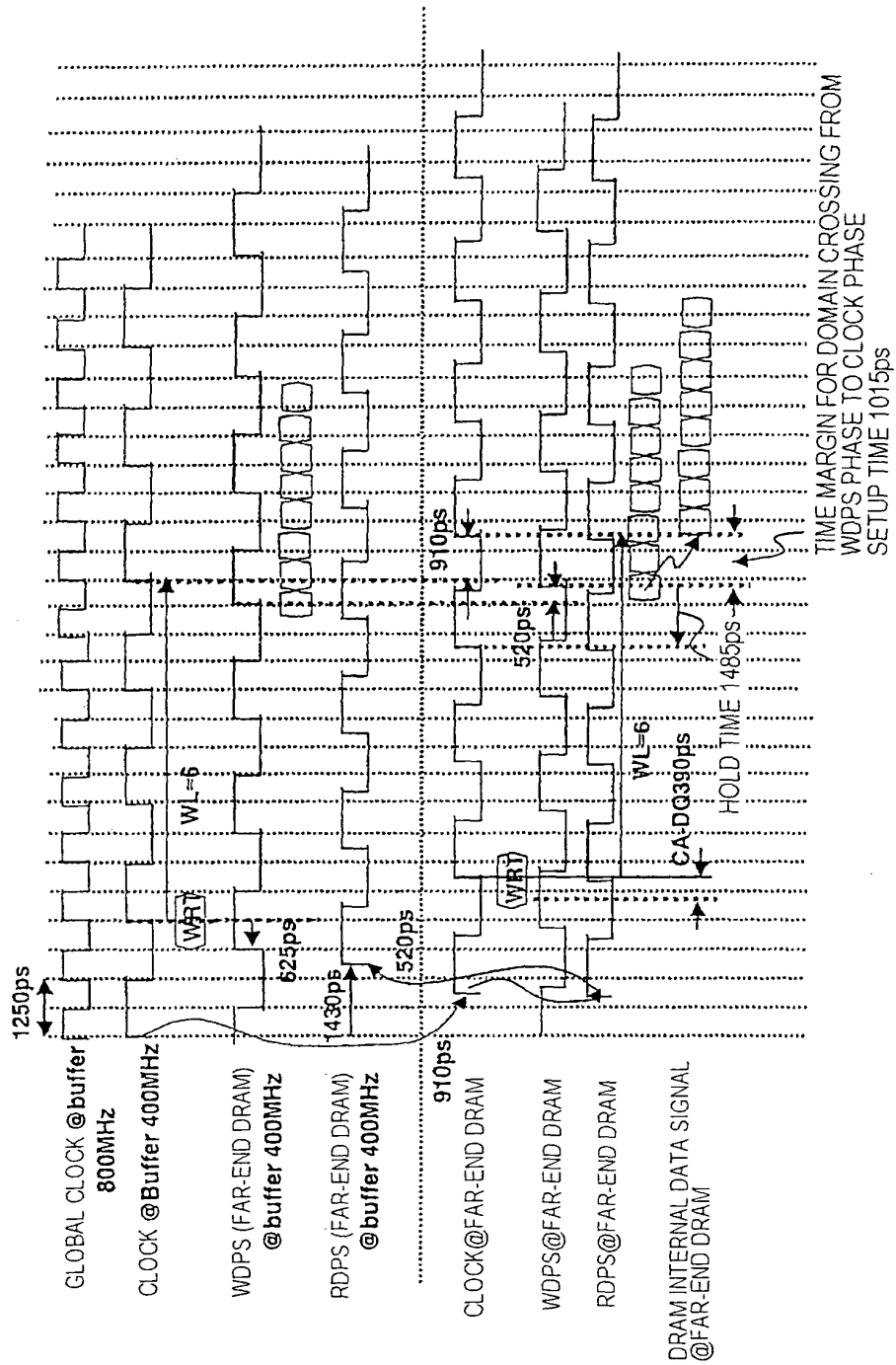


FIG. 56

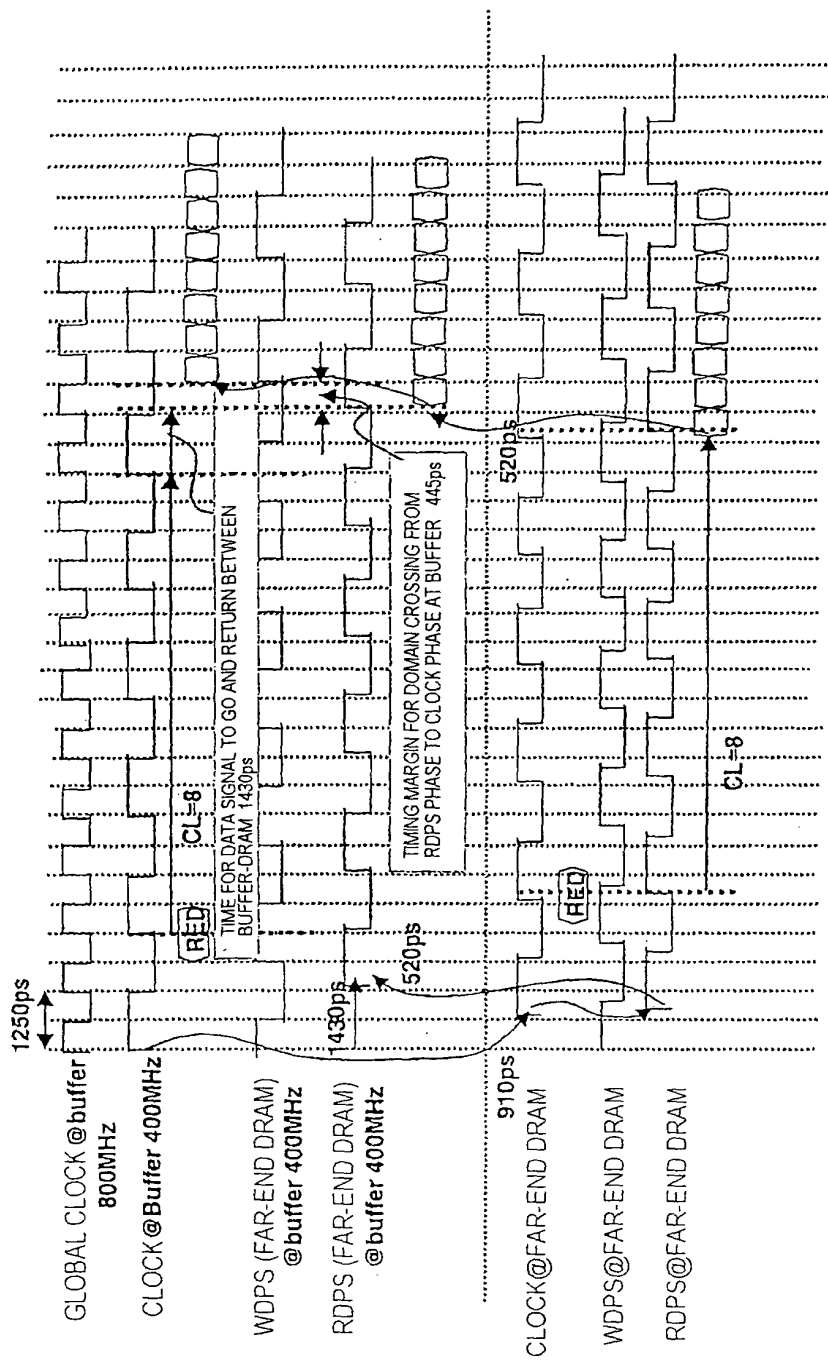


FIG. 57

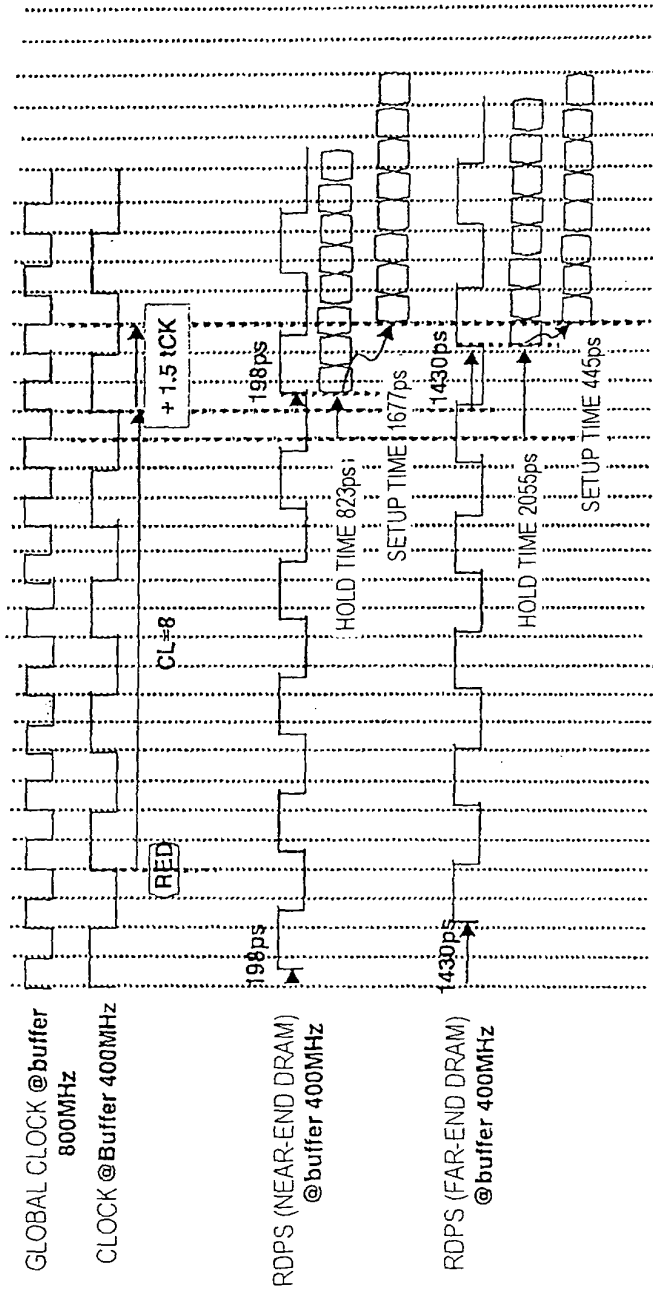


FIG. 58

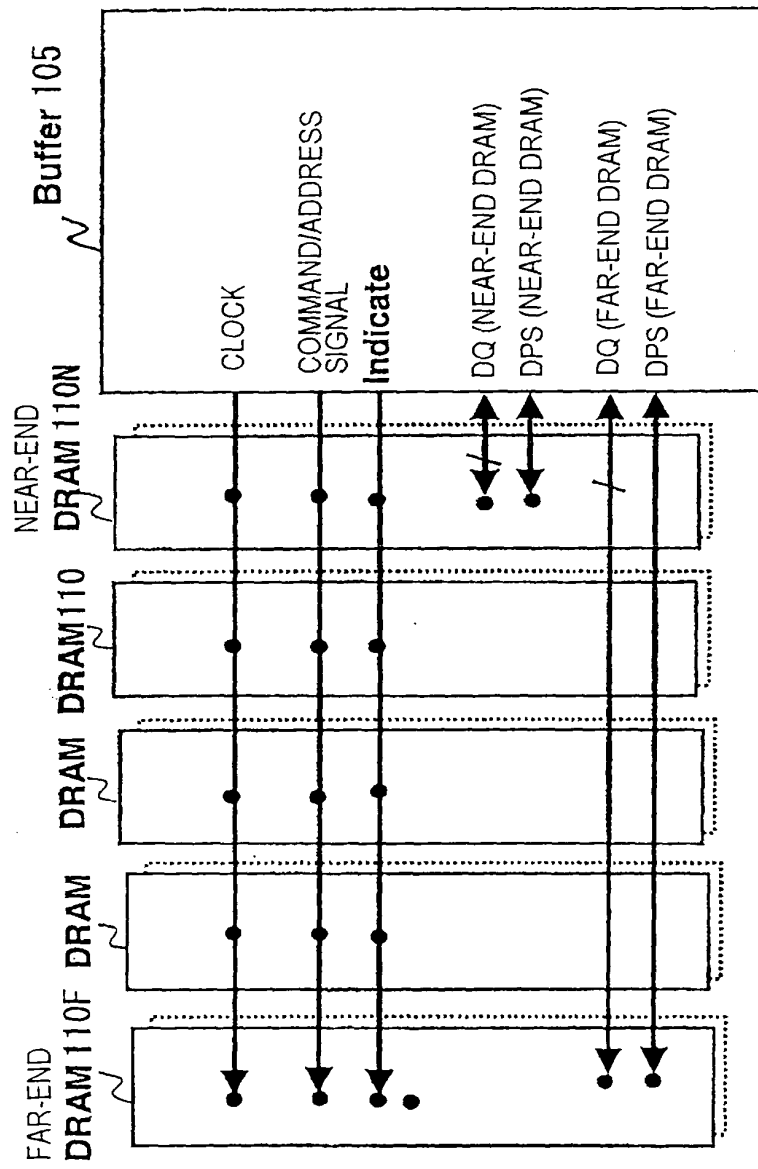
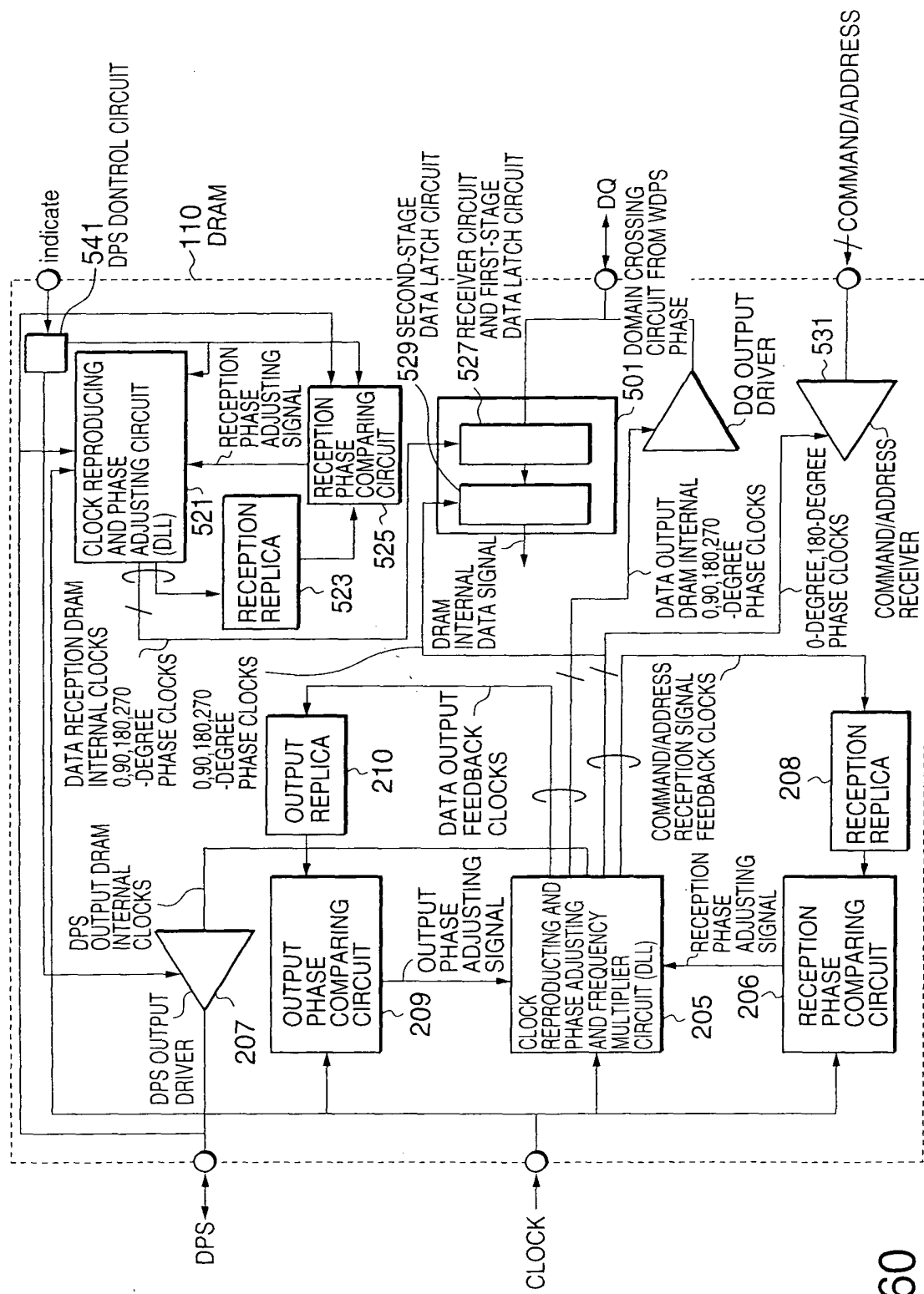


FIG. 59



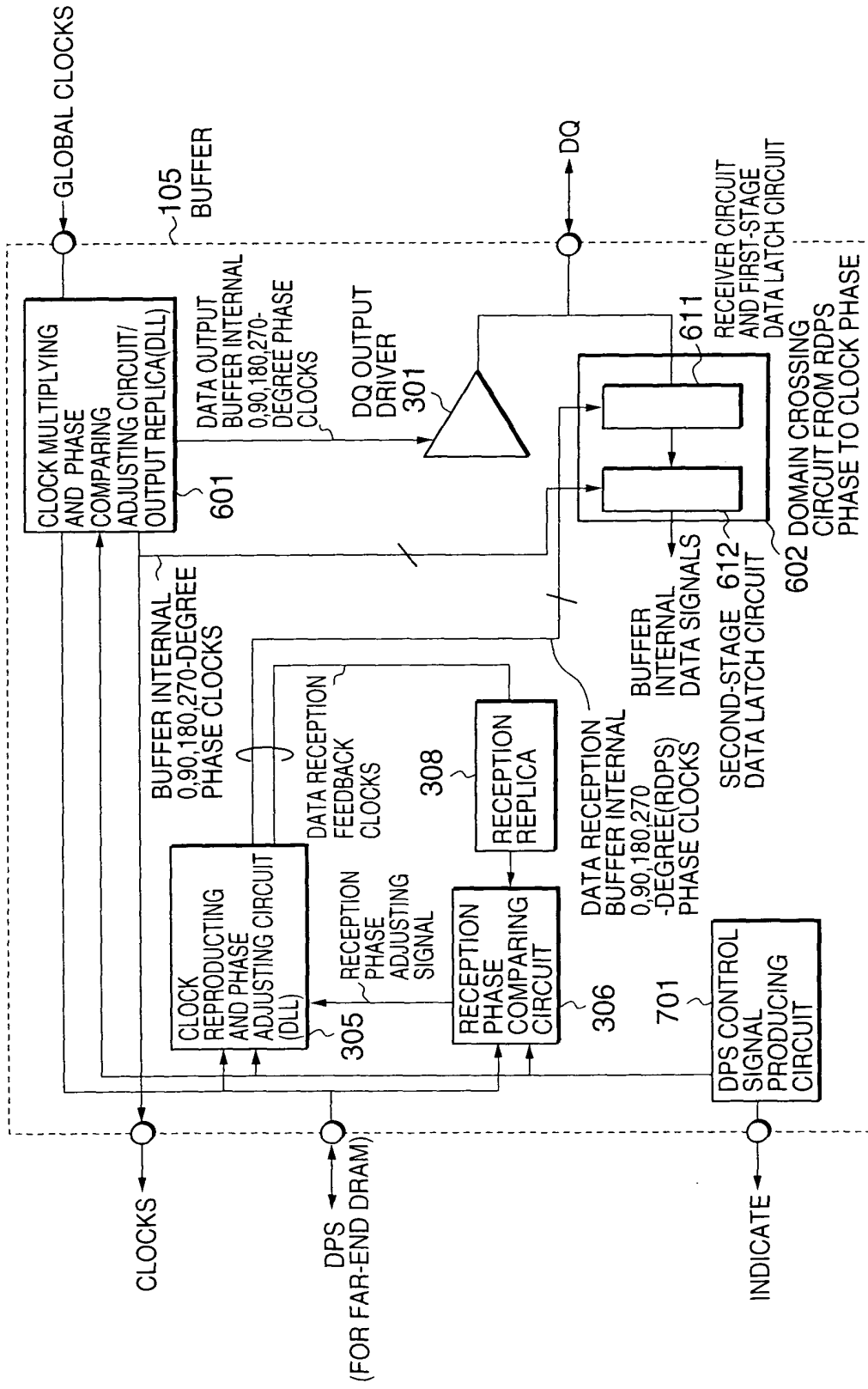


FIG. 61

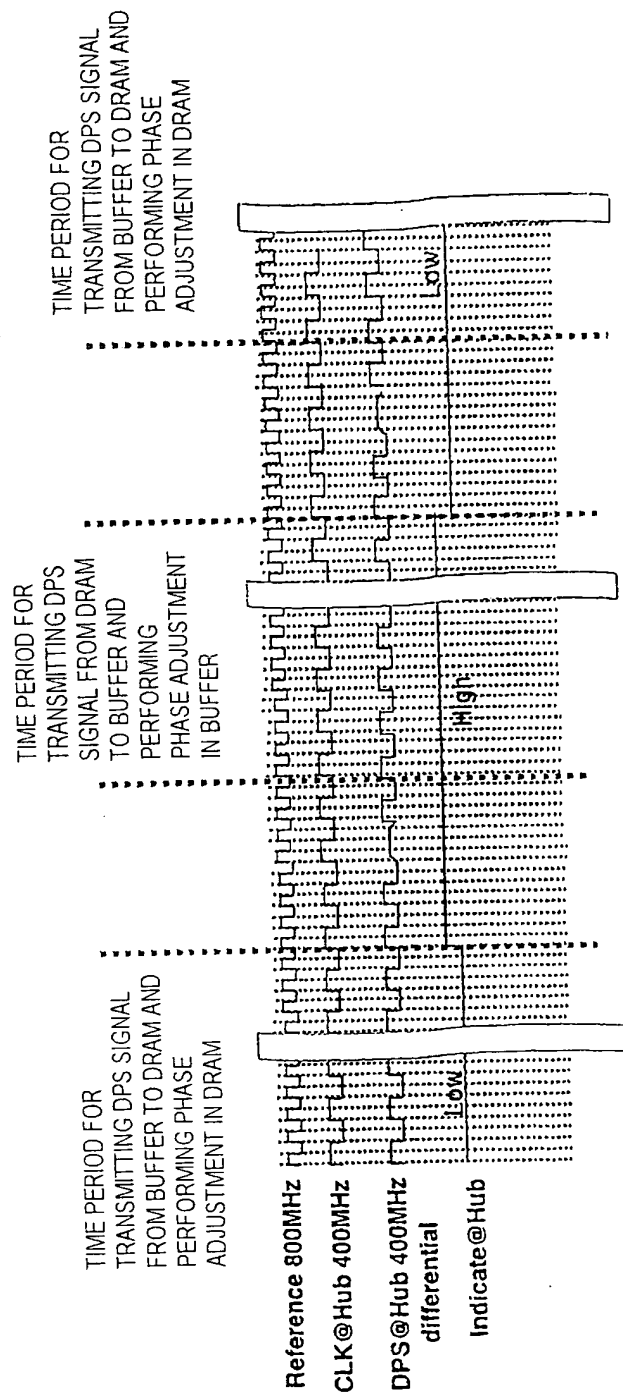


FIG. 62

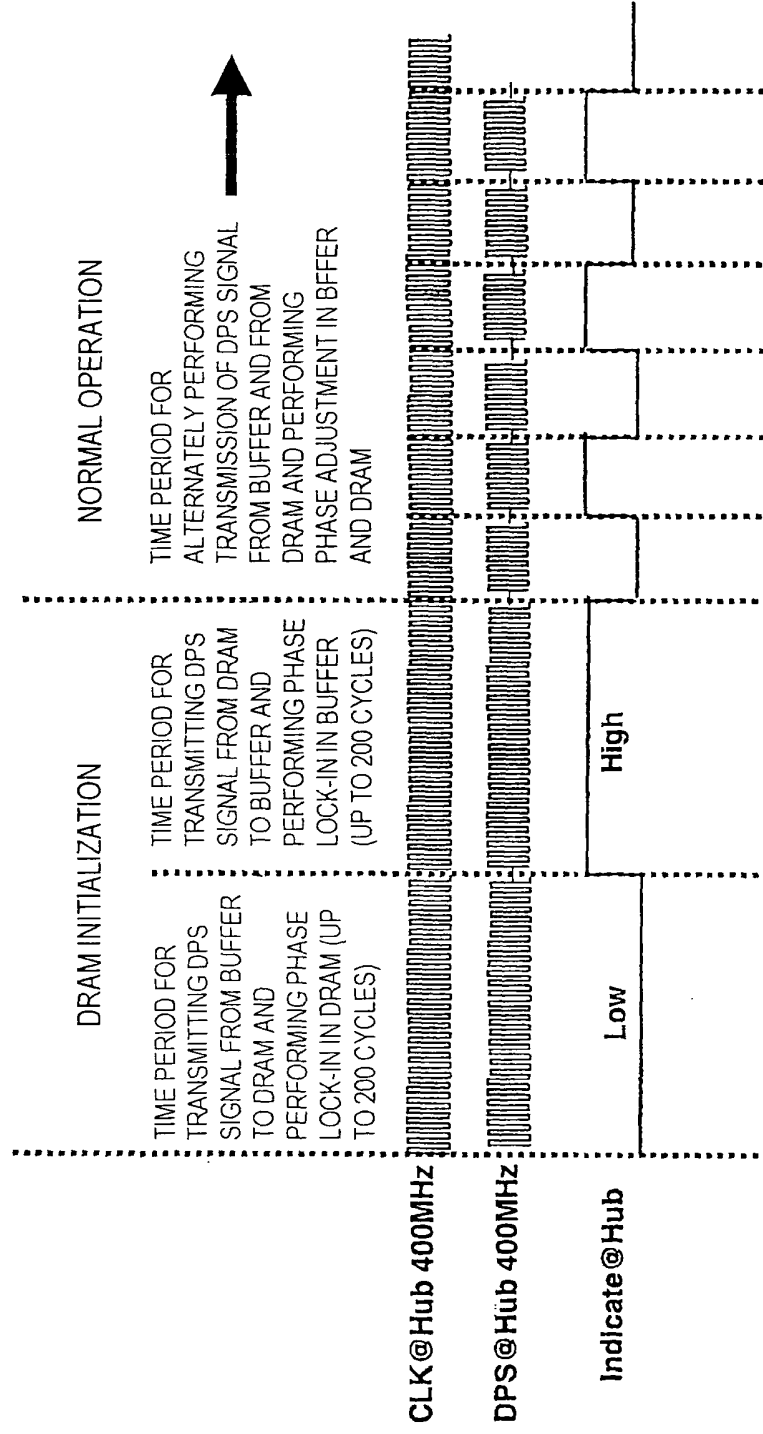


FIG. 63

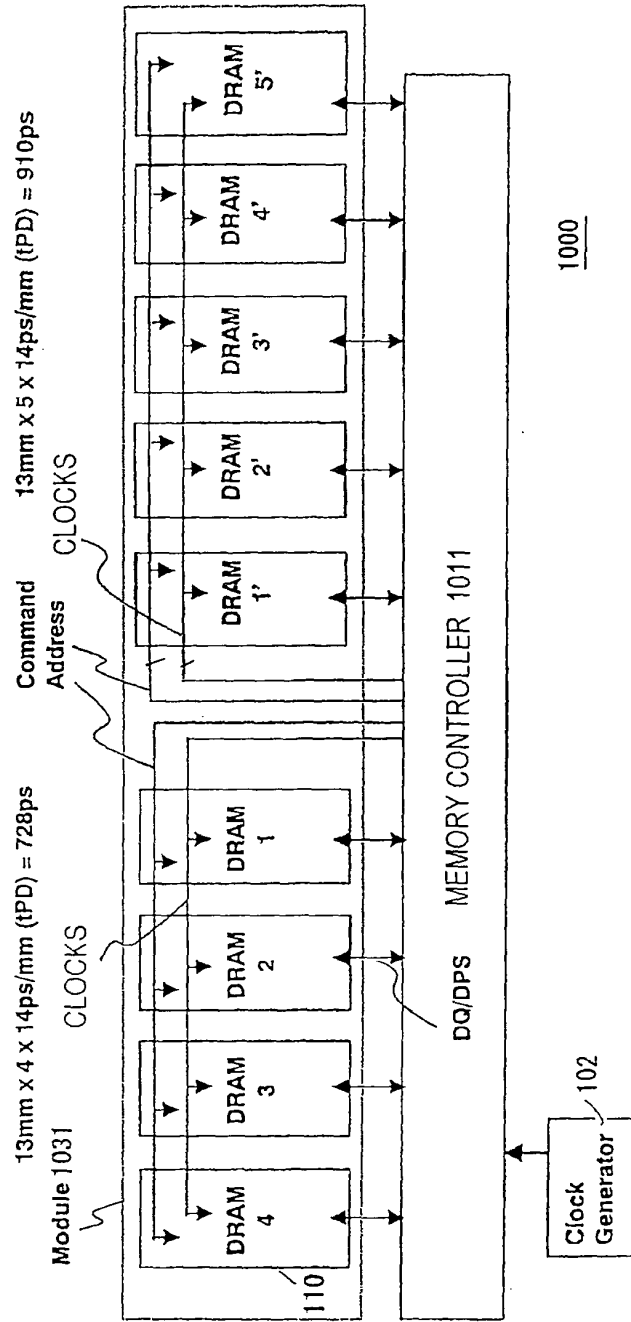


FIG. 64

WRITE OPERATION

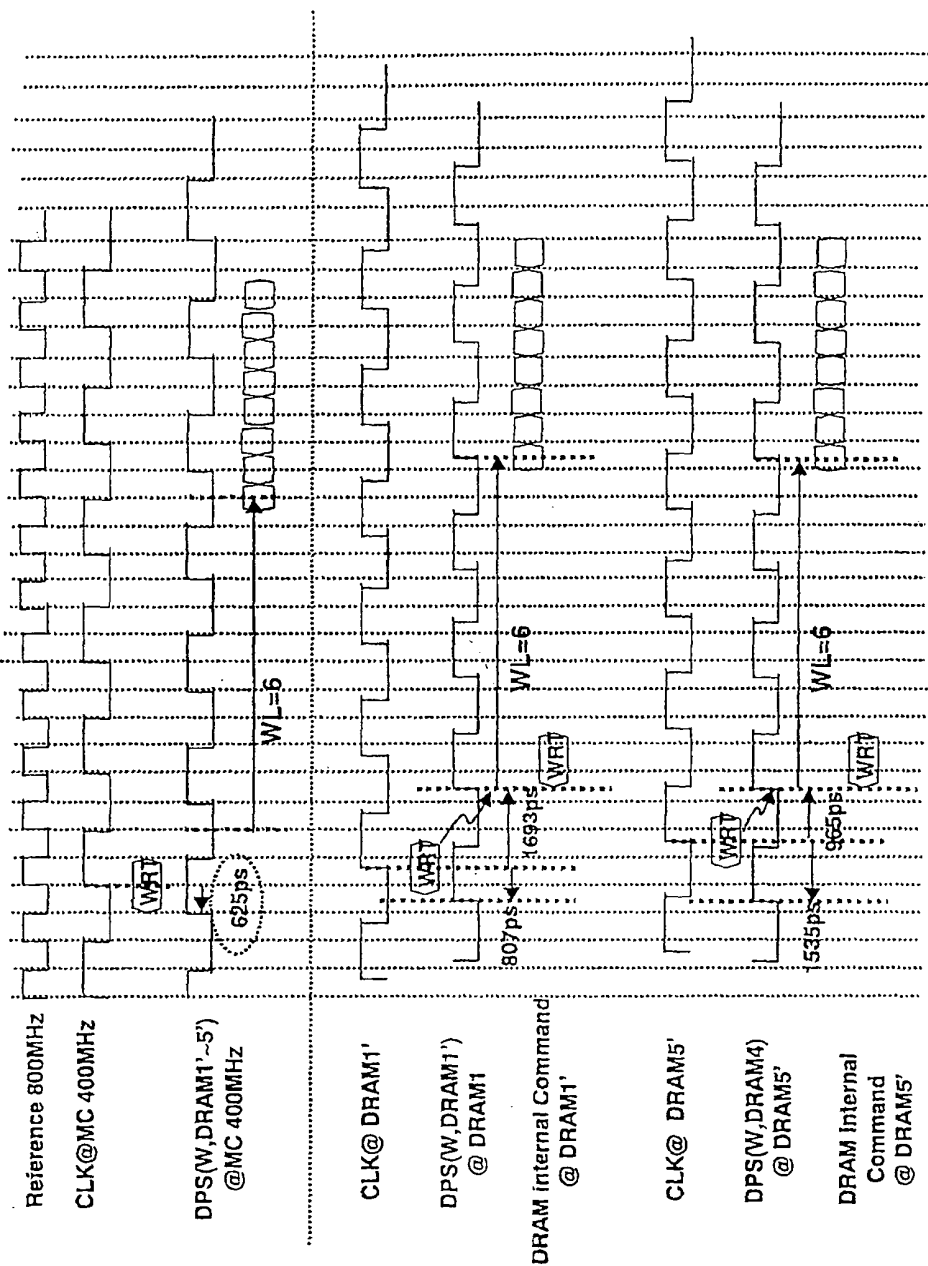


FIG. 65

READ OPERATION

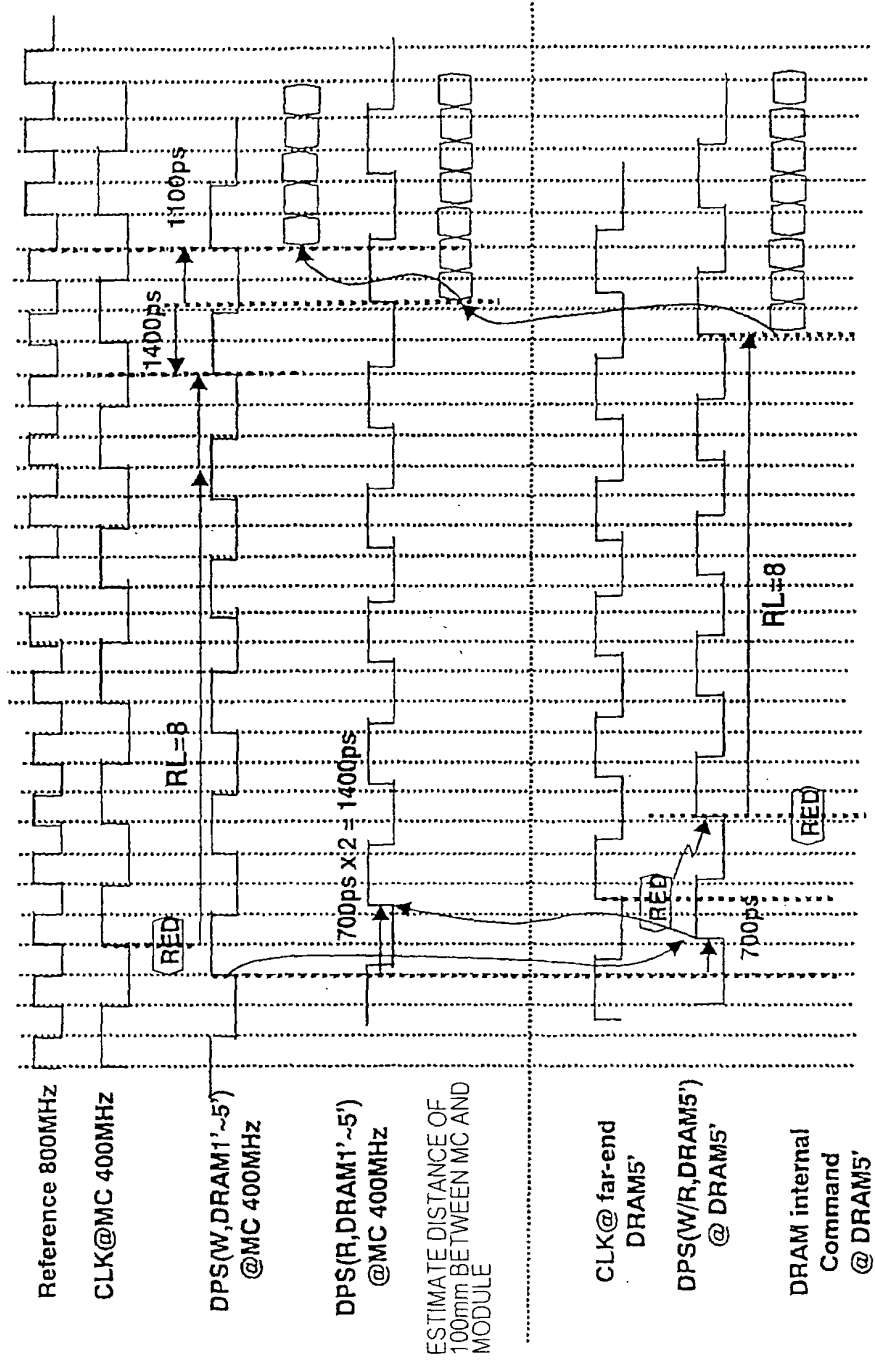


FIG. 66

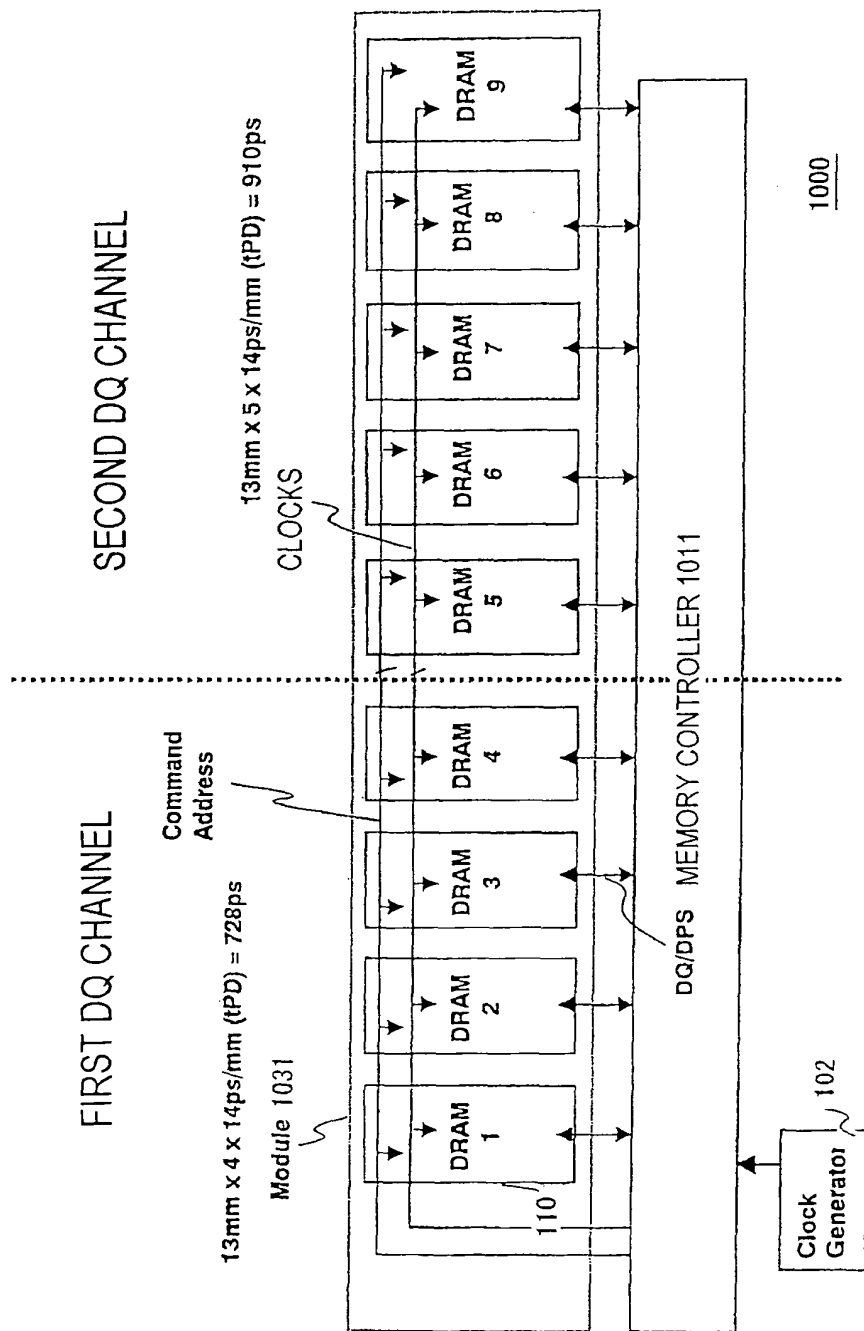


FIG. 67

FIRST DQ CHANNEL WRITE OPERATION

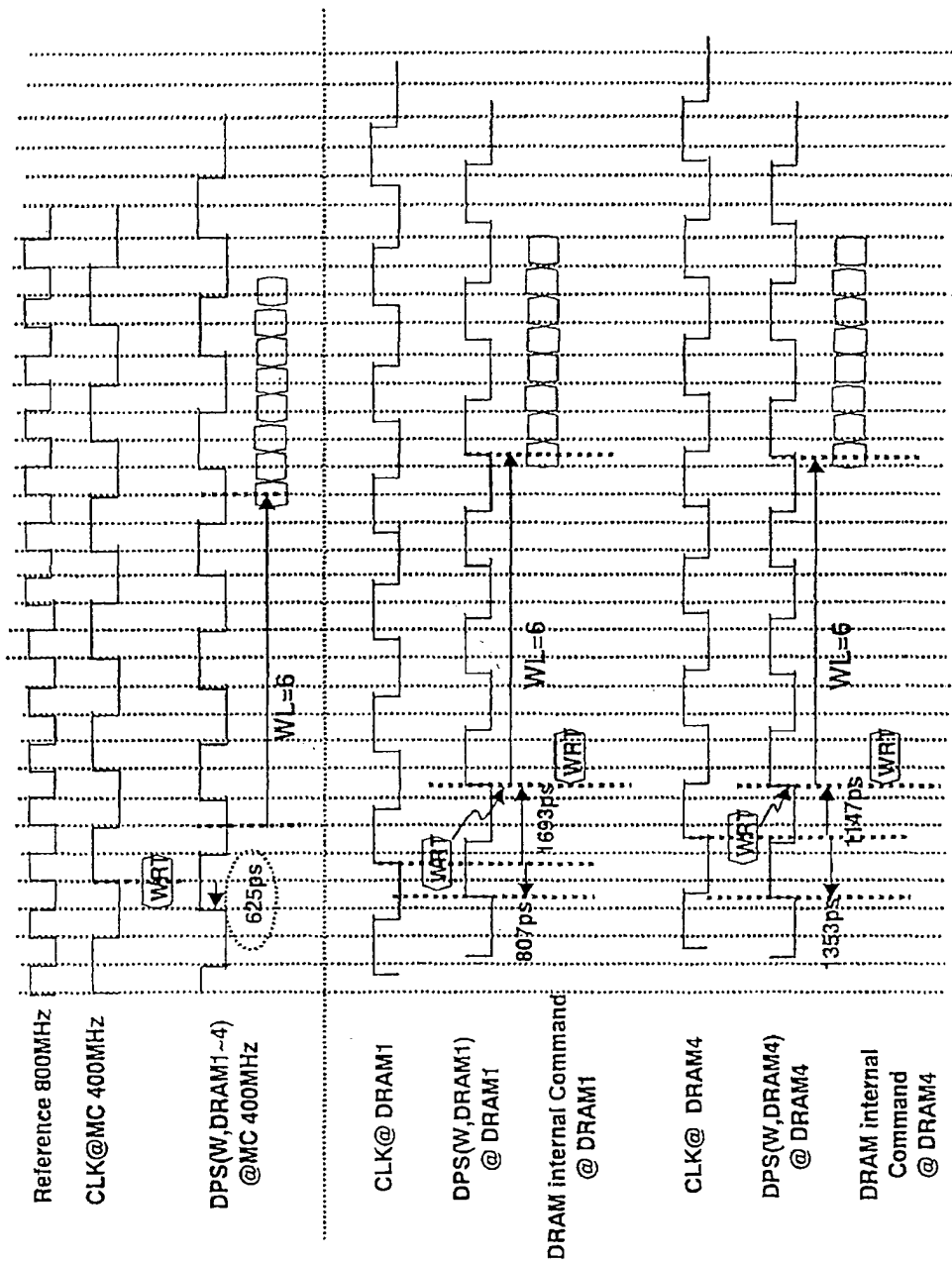


FIG. 68

FIRST DQ CHANNEL READ OPERATION

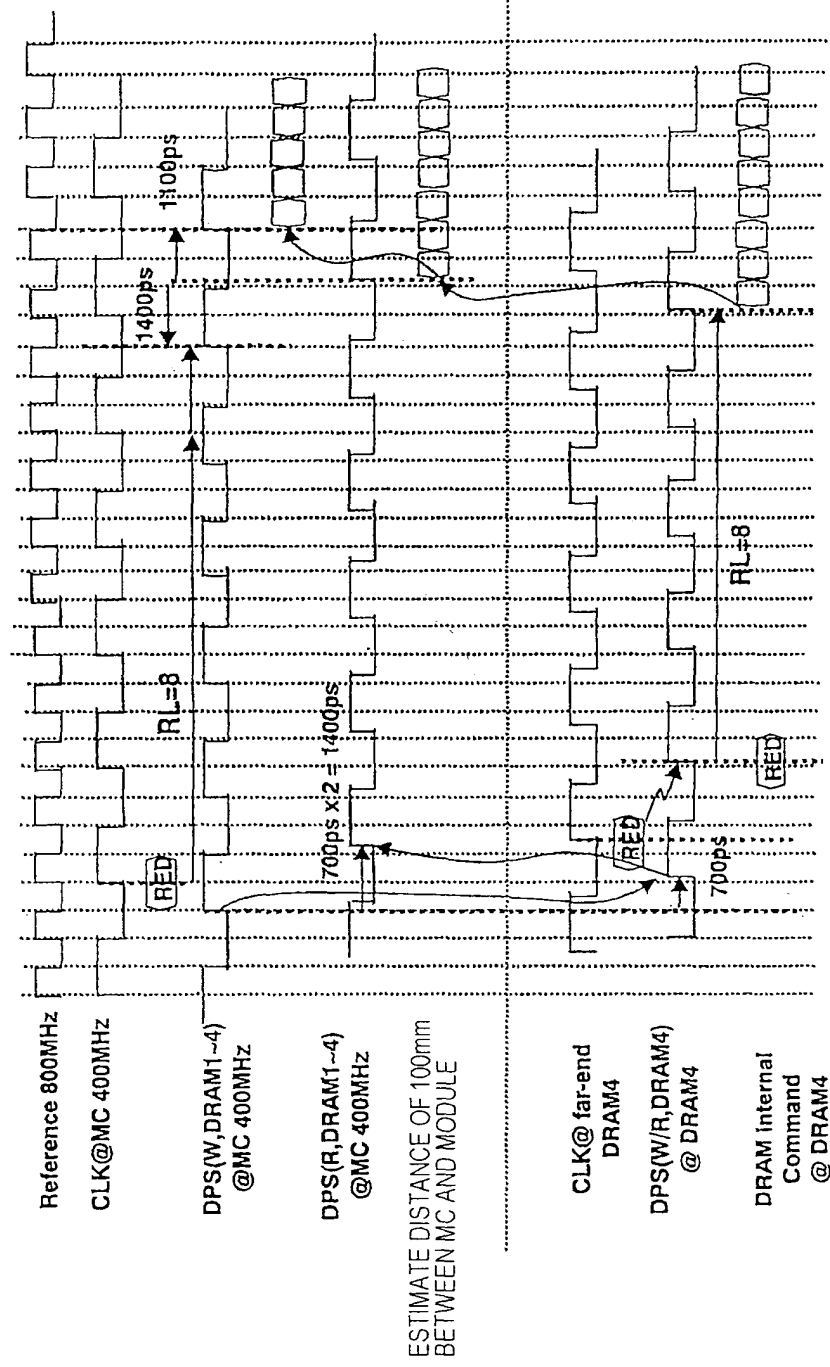


FIG. 69

SECOND DQ CHANNEL WRITE OPERATION

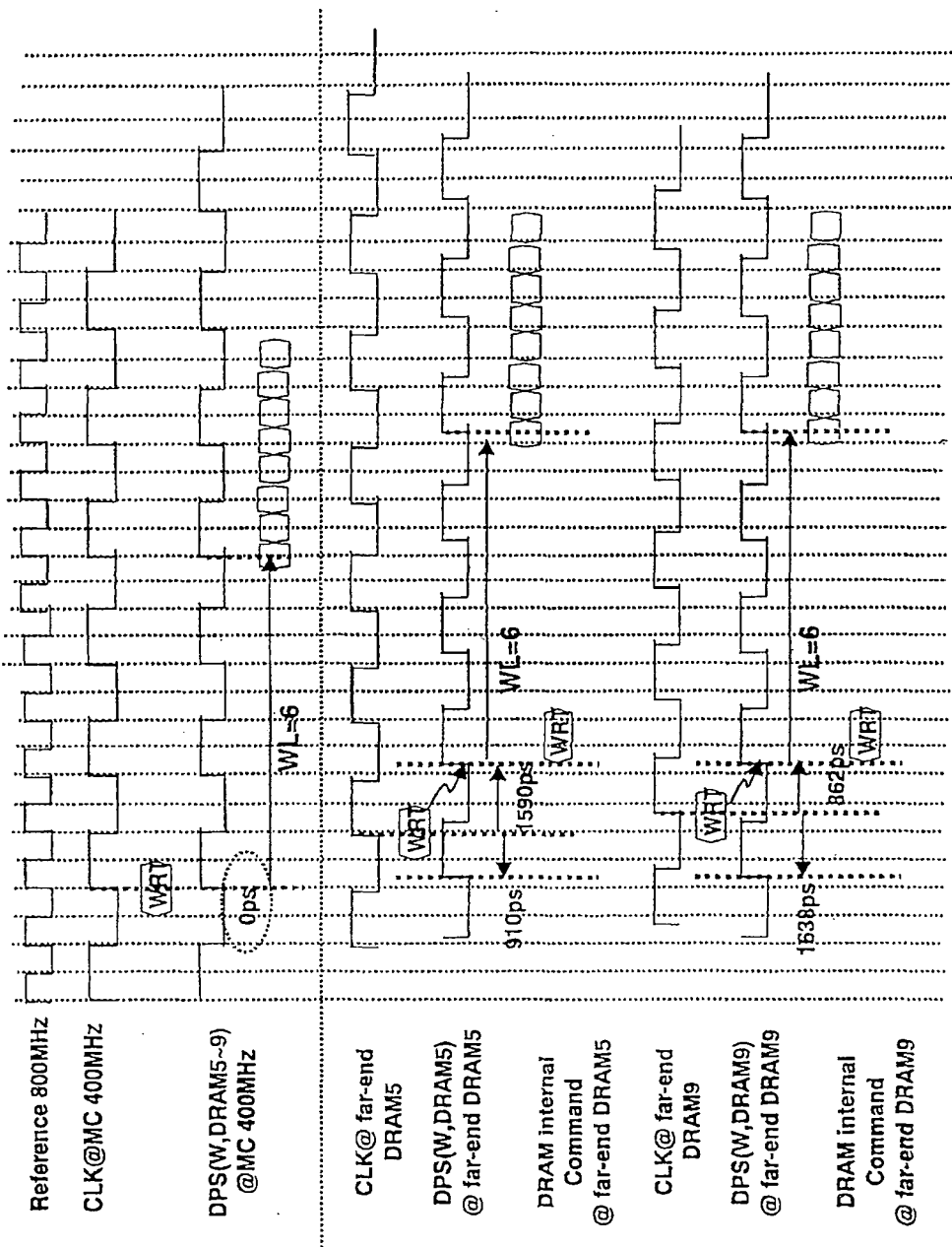


FIG. 70

SECOND DQ CHANNEL READ OPERATION

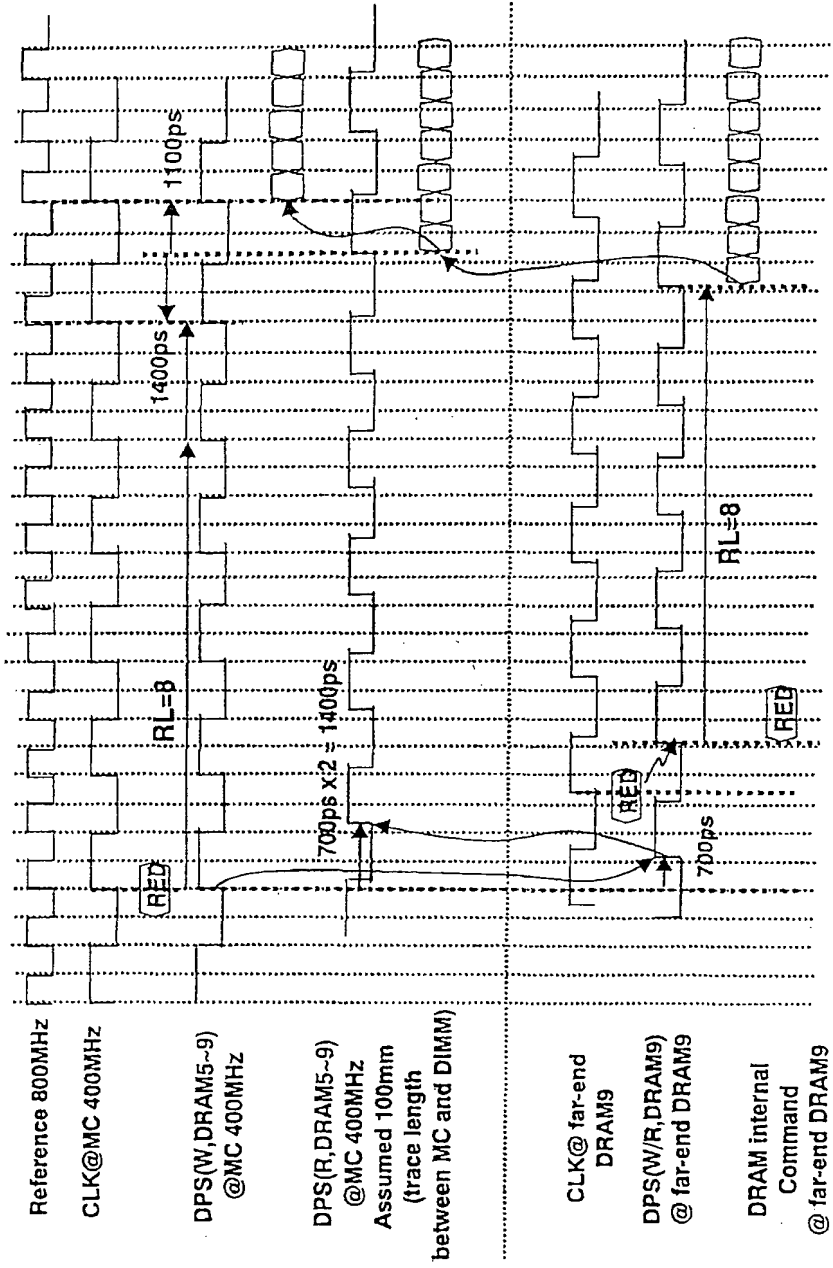


FIG. 71